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Convergence IT Semiconductor Design Technology

- Trends in SoC Design for Wearable Devices UI/UX
- Trends and Tasks of Communication Semiconductor Technology for both Wireless Power Transmission and Medical Communications
- Circuit for wireless power transfer system
- Error Control Methods for Low-voltage, Low-area Embedded Memory
- Virtual Prototype for Early SW bring up & HW/SW co-verification

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Editor' s Comment

Convergence IT Semiconductor Design Technology

Joongho Choi Editor
(University Of Seoul)

Recently, mobile devices hasve been undergoing an unprecedented rate of development and are being applied with converged IT technology at various fields ranging from not only data communication but also automotive, wearable, and medical industries. Such convergence and development of the mobile technology are proceeding on the basis of mobile semiconductor technology that should be the core of hardware as well as software that determines system and its applications.

This special issue consists of five papers written by academic and industry experts addressing the field of mobile semiconductor industry for implementing mobile systems.

The first paper, "Trends in SoC Design for Wearable Devices UI/UX (Jaewook Joo, Seongrim Choi, Jonghun Ahn, and Byeong-Gyu Nam)" introduces the interface technology and trends optimized for wearable devices that have recently come to limelight. Furthermore, it deals with the core SoC design technologies required for putting such UI/UX technology into practice.

Secondly, the paper "Trends and Tasks of Communication Semiconductor Technology for both Wireless Power Transmission and Medical Communications (Jang Hui-don, Na Gyeong-min, and Bien Young-Jae)" deals with content related to technological development and challenges of the next generation's wireless medical semiconductor technology. It introduces the current trends and future challenges for realization of wireless power transfer and data communication technology.

The third paper "Circuit for wireless power transfer system (Moon, Young-Jin and Yoo, Changsik)" introduces the technology for wireless power transmission system, which has begun to be consistently applied to the areas from mobile phones to automotive applications. It deals with the principles, characteristics, and current research trends of various circuits in terms of the core circuit design technology for hardware realization.

Fourthly, the paper "Error Control Methods for Low-voltage, Low-area Embedded Memory (Hoyoung Tang and Jongsun Park)" presents the design technology for embedded memory that can be integrated into chips such as AP, GPU, and DSP, the core components of mobile devices. It explains an appropriate error correction technique under constrained conditions such as hardware space area and consumable energy power consumption.

The final paper "Virtual Prototype for Early SW bring up & HW/SW co-verification (Hyoung ju Kim)" introduces the virtual prototype technique as a new tool for strong competitiveness at the early development stage for hardware and software realization of mobile devices whose complexities have been rapidly increasing.

I would like to express my sincere gratitude for the authors who have provided enormous amount of help for this special issue, in spite of busy schedules. I also wish that this paper's discussion on core semiconductor technology of convergence IT may actively facilitate exchanges of opinion within the relevant fields.

Trends in SoC Design for Wearable Devices UI/UX

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Ⅰ. Introduction

Todays, wearable devices are becoming popular to offer a variety of real-life services as attached to user's body. However, conventional user interfaces (UIs) are not suitable for these devices due to the limited form factors of wearable devices. So, many researches are being conducted to offer more natural and convenient interfaces to the users. Recently, voice recognition, thought recognition, and gesture recognition, shown in 〈Fig. 1〉, are gaining attentions as candidates for the natural user interfaces (NUIs), and low-power design of these techniques is the key to their success on wearable devices.

In this article, we introduce NUI techniques and their low-power implementations to make them suitable for wearable devices.

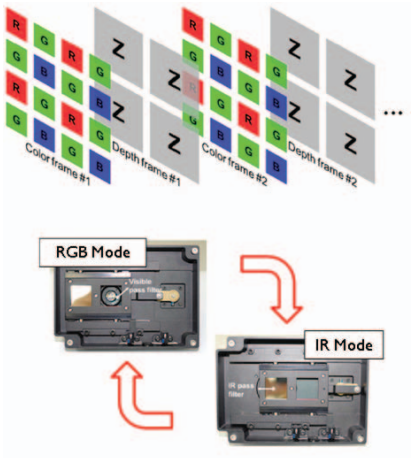
〈Figure 1〉 NUI for Wearable Device

Ⅱ. NUI for Wearable Devices

User interface has started from command line interface (CLI), as shown in 〈Fig. 2〉, and it has evolved into graphical user interface (GUI), and recently, it is evolving into the natural user interface (NUI)[1]. CLI is a traditional input method typing texts into command window by using keyboard, and GUI is an input scheme clicking the graphical icons by using the mouse. In the mobile environment, the GUI has evolved into touch screen based NUI, and in upcoming wearable environment, more intuitive UI schemes using natural body movements is expected to become popular on the devices.

Samsung proposed an IR camera-based 3D vision SoC for gesture recognition interfaces[2]. To reduce area overhead, RGB camera and IR camera are integrated together by adopting the IR filters which are time multiplexed, as shown in 〈Fig. 3〉[2]. On the other hand, UC-Berkeley team proposed an ultrasonic-based gesture recognition SoC to eliminate the power consuming IR camera[3]. It attains 99% of the energy reduction, compared to the IR camera based system. However, the ultrasonic system is very vulnerable to environmental noise and signals can be scattered in other directions, resulting in accuracy loss.

〈Figure 2〉 Development Process of User Interface



〈Figure 3〉 Integration of RGB and IR cameras[2]

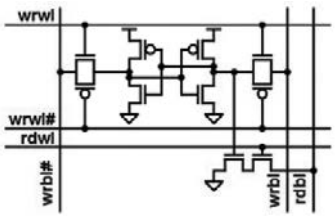
Ⅲ. Low-Power SoC Design for Wearable Devices

The capacity of batteries in wearable devices is severely limited, so ultra-low-power (ULP) circuit design becomes a very critical issue to overcome the limitation of battery lifetime. In this chapter, ultra-low-power design techniques for wearable devices are addressed in terms of the dynamic and leakage power.

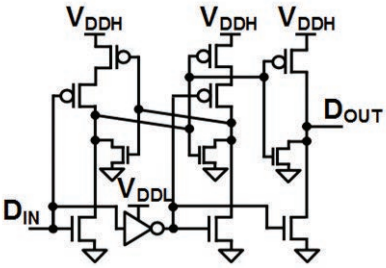
1. Dynamic Power

The supply voltage has a significant impact on dynamic power as the power dissipation depends quadratically on the supply voltage. The dynamic voltage frequency scaling (DVFS) is one of the most effective low-power techniques to adjust the supply voltage and frequency based on the given workload.

Recently, the DVFS expanded to the near threshold voltage (NTV) region to further improve the energy efficiency[4]. In NTV region, SRAM becomes very unreliable thus limiting the voltage reduction of the entire SoC. As shown in 〈Fig. 4〉, low-voltage characteristics of an SRAM can be improved by separating the read and write paths of bitcells and applying differential write



〈Figure 4〉 10-T SRAM bitcell[4]



〈Figure 5〉 ULVS Level Shifter[5]

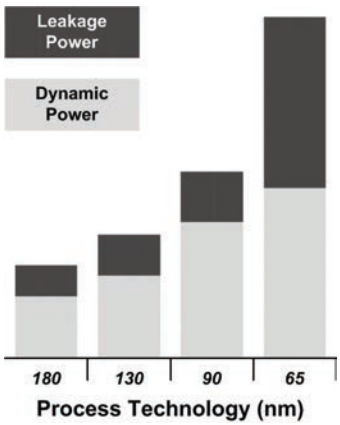
signals by accommodating the PMOS devices on the access paths[4].

Level shifters are also necessary for the interfaces between NTV and nominal voltage regions. The ultra-low-voltage split output (ULVS) level shifter is presented in 〈Fig. 5〉[5], by adopting the PMOS devices to reduce the contention between the pull up and input devices and the NMOS devices to assist the pull down of output node.

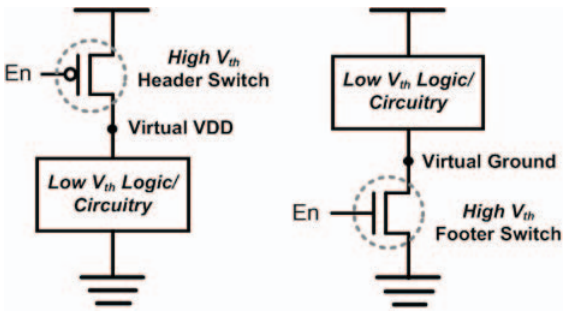
2. Leakage Power

The leakage current has increased drastically with technology scaling and has become a major contributor to the total power, as shown in 〈Fig. 6〉[6]. It is especially critical to the wearable devices which remain in the standby mode for a very long time.

The power gating is one of the most effective techniques to reduce the leakage current[7]. It shuts off the power supply in a sleep mode by turning off the switches between the power rails



〈Figure 6〉 Increase of Power Consumption by Leakage Current[6]



〈Figure 7〉 Power Gating Switch (a) Header (b) Footer[6]

and loads, as shown in 〈Fig. 7〉. PMOS devices are usually adopted for the power switches because of their lower leakage current compared to the NMOS devices. The current surge on the wake-up procedure should be carefully addressed to avoid the electro-migrations and cell flips.

Also, adaptive body biasing (ABB) technique is another candidate for leakage reduction[8]. The ABB controls the threshold voltage by adjusting the body bias of a transistor. It uses the device characteristics that the threshold voltage increases according to the source-to-body voltage (i.e. V_{sb}). However, the effects of ABB are being limited in the latest technology nodes because of the short channel effects prominent in nanoscale devices.

Ⅳ. Conclusion

With the slow-down of smart-phones' market growth, the wearable devices are emerging as the next generation personal computing platform. Wearable devices require more intuitive and natural user interfaces (NUIs) due to their limited form factors. Moreover, battery lifetime is much severely constrained in wearable devices. So, we reviewed the ultra-low-power SoC design techniques to realize the NUI algorithms on wearable devices. We conclude the further studies on the NTV designs are needed to make them suitable for the industrial mass productions.

Acknowledgement

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Trends and Tasks of Communication Semiconductor Technology for both Wireless Power Transmission and Medical Communications

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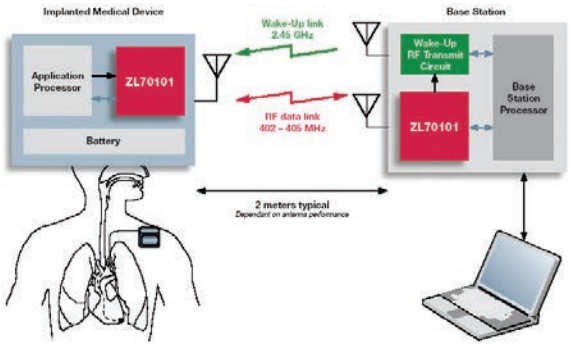
I. Introduction

Today, the medical device industry is growing day by day while the interest for the health is increased all over the world. Recently, smartphones with a pedometer function as well as heartbeat measuring function has been released, and even various remote medical device has been developed.

Due to recent development in wireless communication technology, many devices are implemented with wireless data communication capability. Bluetooth and Wi-Fi are the representative examples classified into WLAN(Wireless Local Area Network), and the needs in this field is continuously growing.

BAN(Body Area Network) is the network configuration defined close to the body in distance, and it must meet the requirement that supports the communication speed from as low as few KBPS to as high as hundreds MBPS while consuming low power. The BAN is being developed as the devices of various types such as the type which is worn on the body and the type which is inserted or implanted into the body in order to collect the medical information for the characteristic numerical value and the state of a patient.

MICS(Medical Implantable Communication System) is one of the standard for communication system in the medical device implanted, and this is classified in the WBAN(Wireless Body Area Network). It is the high speed system of the ultra-low



〈Figure 1〉 ZL70101 System Schematic Diagram (Source: Zarlink)

power wireless frequency operating at 402-405MHz band as recommended by ITU in the International Telecommunication Union Report ITU-R SA.1346.

Some examples that deploy MICS include cardiac pacemaker, cardiac defibrillator and nerve simulator to be used to give a stimulus by implanting into the body, and the drug pump, artificial heart and aids, and implantable sensor for measurement and control. In addition, the capsule endoscope system is used as the representative medical device for MICS.

〈Table 1〉 Purpose of Use in Korea and Other Countries of MICS Frequency Band

Frequency band	Main purpose		Purpose for MICS
	Other countries (ITU Region 1,2,3)	Korea	Korea
402~403 MHz	Meteorological aid earth exploration satellite (Earth-to-Space) Weather satellite (Earth-to-Space) Fixed service Mobile service (except for Aviation movement))	Meteorological aid earth exploration satellite (Earth-to-Space) Weather satellite (Earth-to-Space) Mobile service (except for Aviation movement) K73[*1]	K73A[*2] for MICS
403~406 MHz	Meteorological aid Fixed service Mobile service (except for Aviation movement)	Meteorological aid Mobile service (except for Aviation movement) K73[*1]	K73A[*2] for MICS

[*1]K73: by Fixed service Mobile service (except for Aviation movement) The use of 402~406MHz frequency band is limited to things that are closely related to the meteorological aids service.

[*2]K73A: The frequency band of 402-405MHz is used for MICS. However, it is allowed under the condition that does not give the interference to the Meteorological aid

MICS requirements can be quite challenging as the device is implanted into the body while it must consume very low power to minimize surgical operation for battery replacement. Most implanted devices are operated by a battery of limited capacity, and eventually needs to be replaced through a surgery. While it is costly procedure, it is also painful for the patient. Therefore, it is desireable to have a technology that uses a small amount of battery to elong the period between surgical process. For an actual cardiac pacemaker, its life is expected to be more than 7 years, and in order to implement this, the sleep mode and sniff mode are operated, and it is designed so that very little power is consumed during operation.

The second condition is the size. If it is implanted into the body, the size should be small, and it needs the miniaturization of the chip and parts, and while achieving high efficiency.

And it should have the minimum data transfer rate, and the credibility for operation within a certain distance. In addition, the impact on the body should be minimized. Wireless Power Transfer(WPT) is one of the power transfer techniques currently used. It is possible to transfer power to the place where is difficult to transfer by a conducting wire, as a technology that transmits the power without a medium, not the method by the medium commonly used, and it has the advantage that the user's convenience can be increased, but it has the disadvantage that has lower power transmission efficiency than conventional wired power transmission.

The wireless power transmission technology in WBAN area is almost essential. Currently, as the wireless power transmission technology is gradually developed, it is expected that the size of the device implanted can be also reduced while decreasing the size of the battery. Accordingly, it is expected that the need of surgery for simple battery replacement can be significantly reduced.

In this paper, the authors have investigated two industrial fields, that is, the wireless power transmission and the medical communication semiconductor, and intended to investigate the advantages when both chips will be implemented into single chip and the problems that should be solved.

Ⅱ. Current Situation of Medical Semiconductor Technology

The frequency used in the MICS is 401-406MHz band allocated by ITU- R(The International Telecommunication Union radiocommunications sector) in February 1998. In the United States, the frequency band of 402-405MHz was assigned by FCC(Federal Communication Commission) as a frequency for the MICS equipment in 1999. In Europ, the Wireless communication Committee has allocated the same frequency for MICS under the other name called ULP- AMIs(Ultra Low-Power Active Medical Implants). The Wireless Communication Ministry of the UK and Australian ACA(Australian Communications Authority) have allocated the same frequency for the MICS in October 2002 and October 2003, respectively. Canada and New Zealand have conducted the standardization for the MICS in 2004. New Zealand has allocated 402-406 MHz band.

The UK and Europe belong to Region 1, and the US and New Zealand belong to ITU Region 2 and ITU Region 3, respectively. ITU-R S.A. 1346 research report has recommended so that the meteorological aids service and MICS will share 401-406MHz band.

The recommended conditions for sharing of 401MHz-406MHz band are the wireless frequency with maximum output power of 25uW, the use of the maximum channel bandwidth, and the use of LBT (Listen Before Talk) method by the channel access protocol.

In the case of Korea, 402~405MHz frequency band has been allocated for the MICS under conditions that do not interfere with the meteorological aids service.

The entire system of MICS chip circuit is similar to the general RF circuit. In other words, the circuit parts such as PLL, Amplifier, Modulator/Demodulator, and Filter included in the existing RF circuit, and the components of the sensor and antenna are almost the same.

〈Table 2〉 Current Situation of MICS Technical Specifications

Division	ITU-R	AWF	US	Europe	Japan
Frequency band	401-406MHz	402-405MHz	402-405MHz	402-405MHz	402-405MHz
Power	25uW(EIRP)	25uW(EIRP)	25uW(EIRP)	25uW(EIRP)	25uW(EIRP)
Bandwi	300kHz	300kHz	300kHz	300kHz	300kHz
Interference Avoidance Technique	Interference Mitigation Technique	LBT	LBT	LBT	LBT
Related Regulation	RS. 1346	AWF 3/54	FCC 47 CFR	PART 95	EN 301 839

However, because the circuit that will use only 401-406 MHz band according to the allocation of the MICS frequency should be configured, and it should be mounted inside of the human body, the performance of the antenna and the processor are limited.

Usually, because the size of the battery is very large in comparison with the processor, in order to reduce the size, the battery should be reduced, which is to reduce the power consumption.

Various methods such as the methods that reduce the leakage current and controls the operation method of the overall system have been studied in order to reduce the power consumption of the processor.

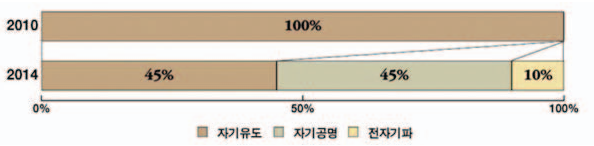
FSK(Frequency Shift Keying) and OOK(On-Off Keying) have been widely used as a modulation method of communication of the MICS. FSK and OOK has become more popular in MICS applications over QAM or OFDM due to its simple struction resulting in smaller implementation size.

One of the most widely used MICS solution is provided by Microsemi Company (old Zarlink Co.), more specificially the ZL70101 series. This chip supports 10 channels with 300KHz bandwidth in the 402MHz~405MHz frequency band that complies with the MICS standard. Moreover, it showed the techniques separating the standby mode and operating mode by Wake-up signal in the 2.45 GHz band.

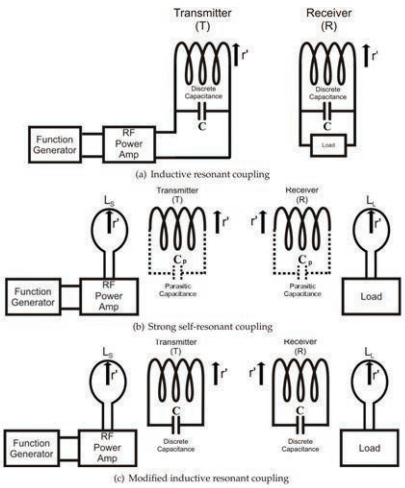
Ⅲ. Current state of Wireless Power Transmission Technology

Wireless power transmission technology is a state-of-the-art technology for the implementation of a complete wireless device. Consumers have been enjoying the wireless devices through battery supply of a number of wireless devices anywhere, while power supply had to be wired for charging. Accordingly, many Companies and Research Institutes have huge interest and investment to completely remove wires of these devices and enable true 'wireless' anywhere. In recent years, the intersts for the wireless energy transmission in the mobile phone and mobile devices fields is becoming increasingly popular in demand day by day.

The wireless power transmission has suggested the possibility that can charge the battery without the connection of wire.The MRI-type medium-range wireless power transmission and the long-distance wireless power transmission



〈Figure 2〉 Prospect of Global Wireless Charger Market by Technique Method



〈Figure 3〉 Prospect of Global Wireless Charger Market by Application

using microwaves among many possibilities are emerging.

For long-distance power transmission using microwaves, the efficiency of power transmission is low and there is the problem that may have a harmful effect on the human body by the IEEE standard (IEEE, 1999). In addition, the wireless power system based on microwave can cause the loss of efficiency if any interrupted object appears in Line of Sight, and if the medium that receives the power is a mobile object, there is the problem that needs a complicated tracking system. Accordingly, the wireless power transmission based on the microwave is suitable to use for the device for military or the space exploration which requires less power. On the other hand, the MRI-type medium-range wireless power transmission is the technology that is harmless to human body and can transmit up to 30m and can be used for the wide range of applications.

One of the important factors to achieve high efficient transmission is to emply a high Q-Factor coil used for a resonator.

Because the wireless charging products which currently is commercialized are based on the magnetic induction method that can charge only within close distance, and the applications provided are limited. The Cahners In-Stat which is a market research company has predicted that currently, only magnetic induction method is commercialized but the magnetic resonance method and the electromagnetic wave method will be gradually commercialized from 2011 and 2013, respectively. According to In-Sat, as the distribution of mobile terminal is increased, it is expected that the market possibility of the wireless charging system will be increased while the discomforts due to different charging option is also increased. According to the investigation results of In-Stat, 44% of mobile phone users have regarded the current charging option is uncomfortable, and 40% of them have said that they can pay $50 for the wireless charging function. It is predicted that the wireless charging system market throughout the world will be able to increase sale of $4.3 billion in 2014, and it is expected that the product cost will be is also consistently declined.

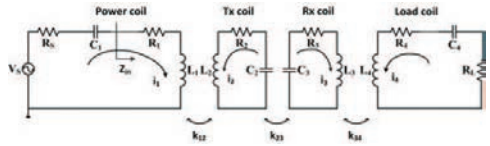
The magnetic resonance-type wireless power transmission is greatly divided into three types. As shown in above figure, there are inductive resonance method, the magnetic resonance method and the magnetic resonance method modified from magnetic resonant mode. The inductive resonance method consists of largely two transmit / receive coil, and the capacitance component mounted in each coil causes resonance, and consequently, the power transmission is achieved. This method has the advantage that coil size is small, resulting in smaller system, while implementation is simple. However, because Q-factor value is relatively lower in comparison with other method, the power transmission efficiency is low, and it shows vulnerable characteristics for the impedance mismatching environment. Next, the magnetic resonance method consists of power, transmission, reception and load coils as a method transmitting power using four coils. This method consists of total four coils, and uses the parasitic capacitance structure, and has the disadvantage that the size of the structure is large because the inductance value should be become larger in order to obtain a lower resonant

frequency.Because the transmitting and receiving coils which cause resonance are away outside of the circuit and does not mount directly the capacitance, it shows high Q-factor characteristics. In addition, because the resonance unit is not directly connected to the power supply and load, it is the method that can be adjusted in the impedance mismatching situation without the resonance frequency variation. Finally, the wireless power transmission technology of the method using four coils, like above the magnetic resonance method, is the method that deliberately mounts a capacitor at the transmission and reception part, unlike the magnetic resonance method. In this case, there is the disadvantage that the efficiency can be decreased owing to somewhat lower Q-factor than the magnetic resonance method, but the size of the structure can be drastically reduced by increasing the size of the capacitance.

〈Fig. 4〉 shows the equivalent circuit of the wireless power transmission system. This circuit was configured to demonstrate the phenomenon indicated by four coils, and these coils can be defined by the combination coefficient. The combination coefficient theoretically has the value between 0 and 1. If all the magnetic waves which is made at the transmitter are delivered to the transmitter, this coefficient can have the value of '1', and reversely, if it is not at all delivered, it has the value of '0'. The coupling coefficient can be defined by the following formula:

$$k_{xy} = \frac{M_{xy}}{\sqrt{L_x L_y}} \qquad (1)$$

Where, Mxy means a mutual inductance between the coil 'x' and the coil 'y', and Kxy has the value between 0 and 1.



〈Figure 4〉 Equivalent Circuit of Wireless Power Transmission

As shown in 〈Fig. 2〉, the power source has an input impedence, and it has the same value as a power amplifier or the input impedance of VAN, and it may have different value according to the situation. Where, RS has the value of general 50ohm. Each coils may be modeled as an inductance L, the parasitic resistance R, and the parasitic capacitance C. This equivalent circuit model enables the efficient approach to the analysis of the characteristics of the wireless power transmission. When Kirchhoff's voltage law (KVL) is applied, the expression on the electric current can be easily obtained, which is as follows:

$$\begin{bmatrix} V_S \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} Z_1 & j\omega M_{12} & 0 & 0 \\ j\omega M_{12} & Z_2 & -j\omega M_{23} & 0 \\ 0 & -j\omega M_{23} & Z_3 & j\omega M_{34} \\ 0 & 0 & j\omega M_{34} & Z_4 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} \qquad (2)$$

Where, Z1,Z2,Z3 and Z4 mean the impedances of each coil. The current of the load coil is calculated from the matrix of (2), and the voltage taking to load can be obtained through the Ohm's law commonly known, which is VL=-i4RL, and the efficiency can be calculated by VL/VS.

The i4 is expressed as follows:

$$i_4 = \frac{j\omega^3 M_{12} M_{23} M_{34} V_S}{ZZZZ + \omega^2 M_{12}^2 Z_3 Z_4 + \omega^2 M_{23}^2 Z_1 Z_4 + \omega^2 M_{34}^2 Z_1 Z_2 + \omega^2 M_{12}^2 M_{34}^2} \qquad (3)$$

Further, such system can be easily interpreted by using the S-parameter. S21 of this system means the power transmission efficiency, which

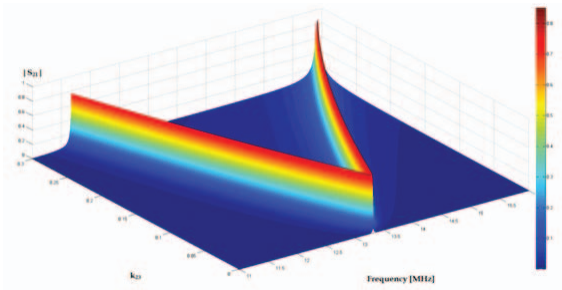
can be represented by the following expression (Sample et al., 2011, as cited in Fletcher & Rossing, 1998; Mongia, 2007):

$$S = 2\frac{V_L}{V_S}\left(\frac{R_S}{R_L}\right)^2 \quad (4)$$

$$|S_{12}| = \frac{2k_{12}k_{23}k_{34}Q_2Q_3\sqrt{Q_1Q_4}}{1+k_{12}^2Q_1Q_2+k_{34}^2Q_2Q_3+k_{12}^2k_{34}^2Q_1Q_2Q_3Q_4} \quad (5)$$

If using the equation above, the equation (5) for the size of S21 can be obtained. This analysis is very efficient to understand the wireless power transmission, and the phenomenons that can be occurred from the wireless power transmission can be proved by using it. Through this analysis, it can be seen that the size of S21 can be determined by only k23 and the frequency. In fact, these principles are the same as already well known. Because k23 is the parameter changed and determined by the distance of two resonators. The more the distance between the resonators is large, the more the value of the mutual inductance become smaller, and the reduction of the overall transmission efficiency is induced. In addition, since the distance of the entire mechanism also grows away by the mismatch between the resonators, it is also led to a decrease in efficiency.

〈Fig. 5〉 shows the formula results graphicallywhen the expected resonant frequency is 13.78 MHz. However, when the coupling coefficient k23 becomes larger than the regular value, the phenomenon that the resonance frequency is divided into two frequencies is occurred, which is called the pole splitting phenomenon. As the distance of two resonators is closer and closer, there are the problems that the reduction phenomenon of efficiency is occurred, and the method for overcoming them will be discussed in a later. The alternate method to verify the system is the method that predicts the efficiency of the power transmission through the equivalent circuit. This confirms the phenomenon that when frequency is divided in accordance



〈Figure 5〉 S21 according to the distance and frequency

〈Table 3〉 Specific Absorption Rate(SAR)

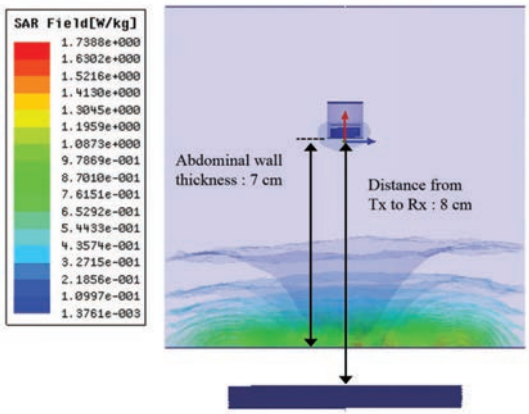
Division		Korea	Japan	US	CENELEC (1)	ICNIRP (2)	IEEE (3)
Frequency range		100kHz~10GHz	100kHz~3GHz	100kHz~600MHz	10kHz~300GHz	100kHz~10GHz	100kHz~3GHz
Ordinary person (W/kg)	Whole body	0.08	0.08	0.08	0.08	0.08	0.08
	Head/Body	1.6	2	1.6	2	2	2
	Limbs	4	4	4	4	4	4
Professional man (W/kg)	Whole body	0.4	0.4	0.4	0.4	0.4	0.4
	Head/Body	8	10	8	10	10	10
	Limbs	20	20	20	20	20	20

1) CENELEC : European Committee for Electrotechnical Standardization,
2) ICNIRP : International Commission on Non-Ionizing Radiation Protection,
3) IEEE : Institute of Electrical and Electronics Engineers.

with the increase of k23. It can be demonstrated via the results predicted in the mathematical expression, and as the distance of two resonators is approached, the value of k23 is increased, and it is soon led to the frequency division. Therefore, in order to increase the efficiency of the power transmission, it needs to supply power by the suitable frequency, or to move the resonance frequency to the desired frequency by using another technique.

Applying the wireless power transmission to a medical body implantable mobile device, existing battery problem can be solved. If the wireless power transmission technology is applied to implantable medical sensors in the body, the more things should be considered in order to apply the technology to mobile devices. The study for the maximum power transmission efficiency similar to the problem in the mobile device should be conducted, and because it is inserted into the relatively constrained space, the size problem should be also further considered. Also, if the stronger electromagnetic waves are consistently radiated, the part that affects on the human body should be also considered.

Each country and the agency have limited the electromagnetic absorption rate, and the standards are the same as in the Table above. Every the agency shows the difference in the frequency range, but they have roughly the same standard in the specified range. In the case of a human body, it should not exceed 0.08 W/kg, which has the most strict criteria because the person can lead to death there if the temperature of human body is increased 1℃. And the body is about 1.6~2 W/kg, and the limb has 4 W/kg which is the lowest standard.



〈Figure 6〉 SAR Simulation Results

If the wireless power transmission technology is taken into the human body, the study satisfying above criteria should be conducted at the same time. The following Figure shows the 3D graph that indicates the absorption rate absorbed into the human body when the power is transmitted into the body by the wireless power transmission technology. The simulation state is the SAR graph in the situation that transmits 0.3 W from the transmission unit to receiving unit, and the point having the maximum SAR value is 1,739 W/kg. The power transmission using a magnetic field among the wireless power transmission technologies has somewhat low the human body absorption rate and a low-risk as the most safe wireless power transmission technology, but it should be carefully studied because it is used to the human body. Also, while it is the field that still is actively researching, and because it has many controversies, the verification experiments such as clinical experiments will be necessarily conducted.

Ⅳ. Medical Wireless Power Transmission Communication Chip

As mentioned above, the body implantable medical devices are subjected to large constraint on the size. Therefore, it is necessary to minimize the size of the device. To achieve this, the size of the battery that occupies the largest volume can be reduced with the use of wireless power transmission

Whereas, If the antenna and the circuit for the wireless power transmission are inserted, the chip size is increased, which is trying to overcome the size problem through the one chip solution of the wireless power transmission circuit and communication circuit. However, for the wireless power transmission, the receive unit must use the HV (High Voltage) process because the deviation of voltage received according to distance, angle and position is large, whereas, for the communication chip, because LV (Low Voltage) process should be used and the power consumption is reduced, the technology that integrates two circuits in one circuit is further needed.

In addition, the voltage interference between the wireless power transmission circuit and communication circuit dealing with power is the task to be resolved.

The medical devices utilizing the wireless power transmission technology and communication chip has the advantage that can solve the existing size constraint problem and the inconvenient that must eject the unit back to charge the battery, but if the wireless power transmission technology and communication chip are coexisted, because the heating problem can be occurred, the solution to it needs. Because it can have a significant effect on the body, and the operating performance can be hindered although the temperature of the device inserted into the body is increased only 1 degree, the temperature sensing for the operation within allowed temperature, and the improvement of the problems above through control circuit techniques are needed. Also, it is required the development of the harmless medical wireless power transmission communication chip through the system implementation that deactivates the operation of chip at the temperature more than the standard value.

Ⅴ. Conclusions

As the medical devices are gradually become state-of-the-art device due to the development of the communication and medical technology, the demands for the patient's safety and convenient is more and more increasing. MICS field is increasingly expanded by the technology that meets these demands. The wireless power transmission field is the technology that gets the attention till mobile phones, household and automotive as well as the medical field, and you can receive several benefits when applied to WBAN. The biggest benefit among them is the miniaturization of devices due to the improvement of mobility and the reduction of battery size. But, because MICS communication technology was not yet widely propagated and the wireless power transmission technology is yet the initial experimental step, the challenges yet to be solved have left a lot. However, if the technology is gradually developed and the development that

thinks the people's convenience and safety is continued, the user's needs are going to increase, and it is expected that the day that everyone will be able to naturally use the MICS device which the wireless charging is possible will come sooner or later.

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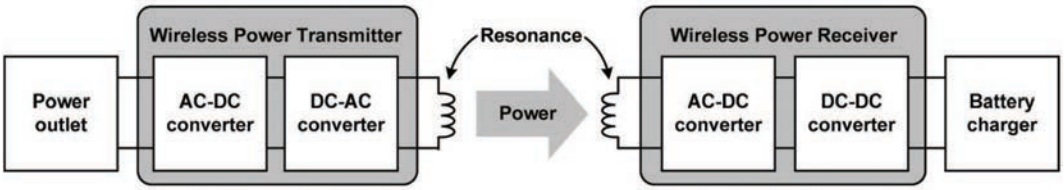
Ⅰ. Introducrion

Recently, efficiency and transmission distance of the wireless power transmission system are significantly improved by applying magnetic resonance technique, and can be widely applied to cell phones, wearable medical devices and electric vehicles. While the efficiency of the wireless power transmission system can be improved by the resonant magnetic coupling, the overall power transmission efficiency is limited by the efficiency of power transmitting and receiving circuitry. Therefore, circuit technique for improving the efficiency of the wireless power transmitter and wireless power receiver to be studied.

The basic structure of the wireless power transmission system is shown in 〈Fig. 1〉. First, the wireless power transmitter receives power from the power oultet, and then transmits power to the resonator. This power is supplied to the wireless power receiver. Received power is changed to suitable DC voltage for the battery charger which supplies power to the battery of the electronic device.

The AC-DC converter inside wireless power transmitter receives the AC voltage of the power outlet, and generates proper DC voltage to DC-AC converter. DC-AC converter is used to amplify the power at the resonant frequency suitable for wireless power transmission system to the resonator by using generated DC voltage from AC-DC converter. It is



〈Figure 1〉 The basic structure of the wireless power transmission system

important to choose a proper structure for the entire wireless power transmission system when designing a DC-AC voltage converter.

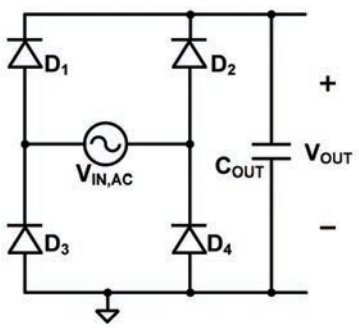
Wireless power receiver receives AC power delivered from resonator, converts it to DC power and supplies it to DC-DC converter. At this time, the frequency of the input AC power is much higher than 50~60Hz of common power outlet, it requires a technique for high efficiency of AC-DC converter. DC-DC converter generates a stable DC voltage suitable for the battery charger. And, an additional consideration for wireless power receiver is the form-factor of the system. Wireless power receiver must be designed smaller size in order to be applied to smaller systems such as mobile phones and wearable medical devices. Also, the wireless power transmission system causes problems such as over-power and over-heat. Therefore, some methods will be introduced to protect wireless power transmission system to ensure a stable operation in situations such as over-power or over-heat.

In chapter 2, section 1, this paper introduces the structure of blocks constituting the wireless power transmitter and a method for obtaining high efficiency, and in section 2, introduces the blocks constituting the wireless power receiver. In section 3 and 4, describe the operation of the battery charger and protection circuit for the stable operation of the wireless power transmitter and receiver. In chapter 3, introduce the development cases of wireless power receiver, and finally, in chapter 4, finish with conclusion.

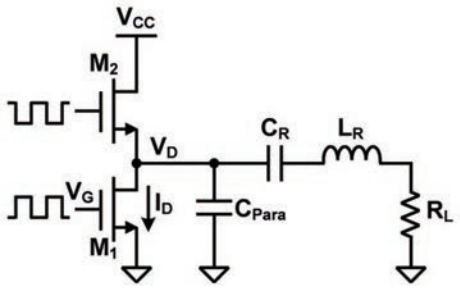
Ⅱ. Research on wireless power transmission system circuit

1. Wireless power transmitter

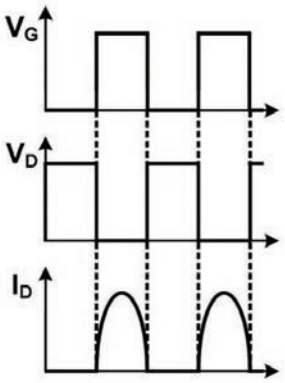
In general, the output frequency of DC-AC converter, that is, the frequency of the resonator is higher than the frequency of 50~60Hz supplied from the power outlet. The frequency of the resonator is ISM (industrial, scientific and medical) band frequency has been deregulated. Accordingly, it does not input the output of power outlet directly to the resonator. It converts the output to a suitable DC voltage required by the DC-AC converter of the wireless power transmitter through AC-DC converter. AC-DC converter can be configured for the user's safety, as a full-wave rectifier, an isolated fly-back or forward converter. The received power of AC-DC converter has a high input voltage and a low



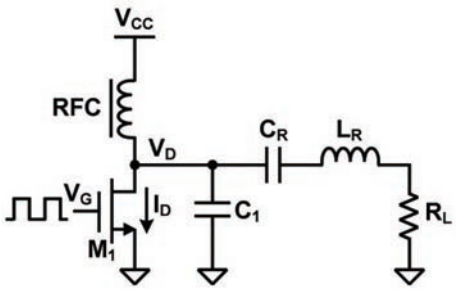
〈Figure 2〉 Full-wave rectifier



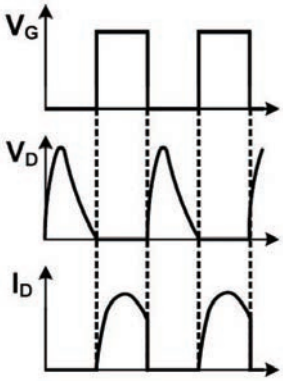
〈Figure 3〉 Class-D power amplifier circuit



〈Figure 4〉 Waveforms of Class-D power amplifier



〈Figure 5〉 Class-E power amplifier circuit



〈Figure 6〉 Waveforms of Class-E power amplifier

frequency unlike AC-DC converter in wireless power receiver will be described in section 2. As shown in 〈Fig. 2〉 therefore, it is possible to expect a high efficiency by applying a full-wave rectifier which is composed of four diodes and one capacitor. Then the AC-DC converter is possible to configure a high efficiency AC-DC converter by applying transistor having a large size and a good performance, flyback and forward control integrated circuit because the size limitation of wireless power transmitter is relatively low that is different from wireless power receiver.

In contrast, DC-AC converter requires a variety of research because it has different efficiencies depending on structure and frequency. DC-AC converter transmits power to the load by amplifying the input AC signal using the DC voltage generated by AC-DC converter, for that reason it is also called power amplifier. The power amplifier which is generally known, is divided into linear power amplifier: class-A, -B and -AB, switching power amplifier: class-D and -E. Linear power amplifier is good to use in cases of modulating amplitude and phase and has good linearity. Power loss caused by overlap section between drain-source voltage of the transistor and the electric current running through transistor, therefore, it is difficult to obtain a high efficiency. In general, when transmitting power wirelessly, it is the most important performance goal to obtain a high efficiency without modulating amplitude or phase. Therefore, switching power amplifier that can be expected a high efficiency has to be applicable to wireless power transmitter.

〈Fig. 3〉 and 〈Fig. 4〉 are, respectively, a circuit and waveforms of class-D power amplifier. 〈Fig. 5〉 and 〈Fig. 6〉 are, respectively, a circuit and waveforms of class-E power amplifier. Both of class-D and class-E power amplifier have no overlap section between drain-source voltage of the transistor and the electric current running through transistor, therefore, power loss does not occur, thus, are possible to obtain a high efficiency. Class-D power amplifier can be advantageous of drain-source voltage of transistor is small compared to class-E power amplifier. In the case of transistor to withstand high voltage, impedance is higher than transistor to withstand low voltage, therefore, class-D power amplifier with low voltage burden can be advantageous in terms of conduction loss.

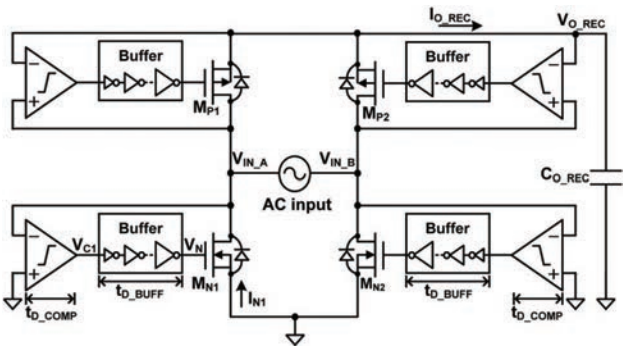
However, in the case of class-D power amplifier, it requires a non-overlap generator to prevent electric leakage which may be happened when power supply voltage VCC and ground voltage GND are shorted due to M1 and M2 transistors closed at the same time. In addition, the parasitic capacitor CPara of transistor has to be charged and discharged in every single switching cycle, which causes the switching power loss and reduces the efficiency. In contrast, class-E power amplifiers can be expected higher efficiency because it is possible to use a parasitic capacitor component. And in the case of class-D power amplifier, is necessary to drive two transistors and thus causes twice of gate driving loss.

The switching and gate driving loss described above of power amplifier is proportional to the frequency. Therefore, at low frequencies, class-D power amplifiers may have a higher efficiency, and at high frequencies, configuring DC-AC converter by using the class-E power amplifier can obtain a high efficiency. As a result, when selecting a power amplifier, it is preferable to be selected by comparing the efficiency of the two power amplifier depending on a frequency and a voltage as a target in a wireless power transmission system.

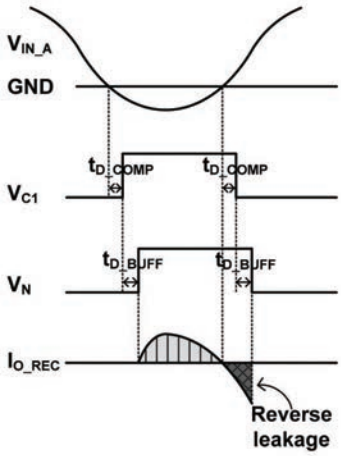
2. Wireless power receiver

As described in section 1, AC-DC converter may be considered a full-wave rectifier circuit composed of four diodes and one capacitor as shown in 〈Fig. 2〉. However, unlike the situation of AC-DC converter of the wireless power transmitter, a small voltage and a high frequency of signal to be input will be large negative effect on efficiency. For example, suppose the AC input voltage is 100VPK-PK and the voltage drop of the diode is 0.7V, it is possible to obtain a power conversion efficiency of 97.2%. However, suppose the AC input voltage is 10VPK-PK, efficiency is lowered to 72%. Besides, efficiency will be reduced by reverse recovery time of the diode. Reverse recovery time is a state that the current cannot be changed to 0A immediately when the condition of the diode changed from the forward bias to the reverse bias. After reverse bias, the diode current temporally flows from the cathode to the anode by the charge storage of minority carriers. Generally, the P-N diode is difficult to apply to wireless power transmission system is operated at a few MHz or higher because it has dozens or hundreds of a value of ns.

Therefore, AC-DC converter of wireless power



〈Figure 7〉 The structure of active rectifier



〈Figure 8〉 The waveform of active rectifier

receiver may be configured by applying a schottky diode which voltage drop is smaller than P-N diode and reverse recovery time only takes dozens or hundreds ps. To remove the voltage drop of schottky diode, MOS transistor that has impedance close to approximately 0 Ω can be used.

〈Fig. 7〉 and 〈Fig. 8〉 are the structure and the action waveform of active rectifier respectively. It requires a comparator to operate a transistor as a diode and buffer to drive MOS transistors.

If node VIN_A voltage is lower than GND voltage, the output of the comparator becomes high, thereby turn on the transistor via a buffer, conversely, if node VIN_A voltage is higher than GND voltage, turn off the transistor to be operated as a diode. Generally, grow the size of the transistor to lower the impedance for increasing the efficiency of active rectifier, thus, the transistor has a large gate capacitance. Consequently, it operates the transistor by using the driving buffer without connecting the output of the comparator to a gate of the transistor directly. Efficiency of the active rectifier can be defined by the following formula.

$$Efficiency = \frac{V_{OUT} \cdot I_{OUT}}{V_{OUT} \cdot I_{OUT} + P_{LOSS,cond} + P_{LOSS,driv}} \quad (1)$$

$$P_{LOSS,cond} = 4I_{N1,RMS}^2 \cdot R_{ON} \quad (2)$$

$$P_{LOSS,driv} = 4C_{gate} \cdot V_{O,REC}^2 \cdot f_{RES} \quad (3)$$

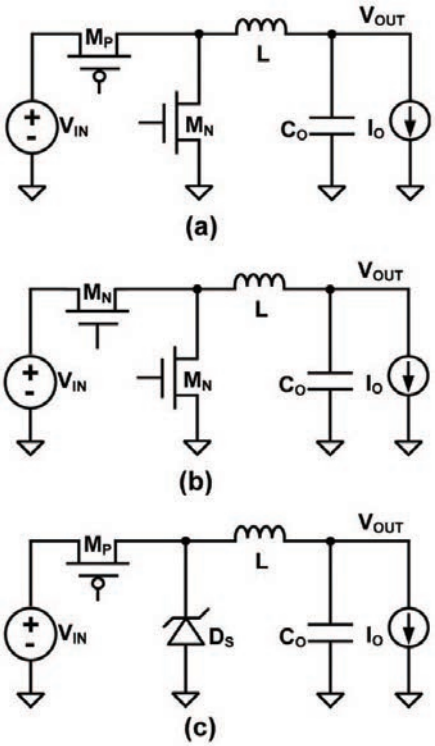
In the above formula, PLOSS,cond means the conduction power loss, PLOSS,driv means the driving power loss, RON means an impedance of MN1, Cgate means the gate capacitance of the transistor and fRES means the resonance frequency. For simplifying the efficiency analysis, the power loss due to the parasitic capacitance between each drain-source of the power transistor and the power loss due to the DC resistance of the inductor are omitted. To increase the efficiency of the active rectifier by using the method of reducing the conduction power loss, the impedance of the transistor should be reduced. In general, there is a way to reduce the impedance is increasing the width of the transistor. However, it increases the gate capacitance, whereby driving power loss will be increased. Conversely, if the size of the transistor is designed to be smaller in order to

reduce the driving power loss, it increases impedance of the transistor, conduction power loss will be increased either. Therefore, in order to obtain an optimal efficiency of the active rectifier, it must be designed to minimize the sum of the conduction and driving power loss via several simulations.

Not only power losses of conduction and driving power previously described but also reverse leakage current caused by time delay of the comparator and driving buffer, are causes of lowering the efficiency. As shown in the waveform of 〈Fig. 8〉, when a node VIN_A voltage becomes lower than GND voltage, after a time delay of about tD_COMP, this will be inputted to the driving buffer, once more, after a time delay of about tD_BUFF, then on-off operation of the transistor will be performed. At this time, reverse leakage current is generated by the late off operation. The generated reverse leakage current causes much worse the efficiency of the active rectifier, therefore, a number of researches for preventing the reverse leakage current are published[3-5].

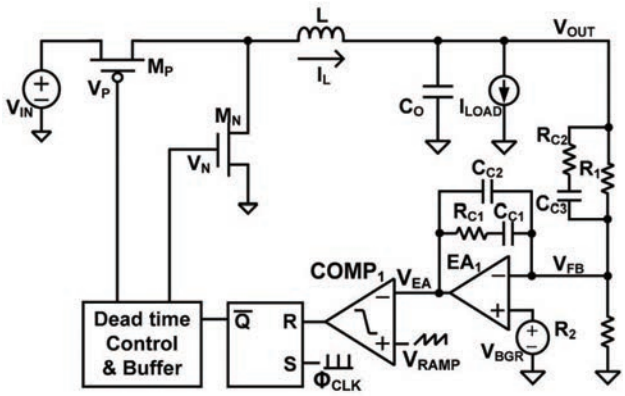
If reverse leakage current is prevented by circuit technology and the sum of the conduction and the driving power loss is the lowest, it is not always active rectifier has a higher efficiency than the rectifier which is configured by applying schottky diodes. The reason for this is the driving power loss is proportional to the resonant frequency. If the resonant frequency is low, active rectifier can have a high efficiency, on the contrary, if the resonant frequency is high, rectifier consisting of schottky diodes can have a higher efficiecy than active rectifier. Therefore, should get the best efficiency by selecting a rectifier that is suitable to the resonant frequency. And wireless power receiver requires a DC-DC converter. The output of AC-DC converter does not directly input to the battery charger because generally the battery charger requires a constant voltage. On the contrary, the output voltage of the AC-DC converter can be varied by factors such as changes in the distance between a wireless power transmitter and a receiver. If the distance between a wireless power transmitter and a receiver is far, the input voltage of AC-DC converter will be lower by a decrease in the efficiency of the resonator, which results the output DC voltage will be lower. Therefore, DC-DC converter is required to supply a stable output voltage to the battery charging circuit DC-DC converter is generally divided into a linear DC-DC converter such as a low-drop-out regulator and switching DC-DC converter. Linear DC-DC converter has the advantage of the form-factor compared to switching DC-DC converter, however, it has a lower efficiency. Therefore, it is not suitable for wireless power transmission system. Therefore, this paper describes switching DC-DC converter by placing emphasis on the high efficiency.

The first thing to be considered at design of switching DC-DC converter is which an element is good for a power transistor. High side switch is placed between the input voltage and the inductor, and low side switch is placed between the power inductor and the ground. In general, impedance of power pMOS transistor has a large impedance more than nMOS power transistor. Therefore, as shown in 〈Fig. 9(b)〉, the highest efficiency can be achieved when using the nMOS power transistor for both side switches. However,



〈Figure 9〉 The structure of a power transistor of the switching DC-DC converter

it requires voltage higher than the input voltage to drive nMOS power transistor used as a high side switch. It is requires a bootstrap driving circuit to do this. However, generally a bootstrap driving circuit requires a turn-on operation of low side more than once for the first time. If the fully turn-on operation is required because an input voltage is low, a problem should have periodically charge the capacitor of the bootstrap driving circuit may occur. And, since bootstrap circuit requires a single external capacitor, if it is necessary to decrease form-factor of the overall system, the high side switch can be replace with pMOS power transistor, as shown in 〈Fig. 9(a)〉. As shown in 〈Fig. 9(c)〉, schottky diode that has lower voltage drop can also be used as a low side switch. However, unlike AC-DC converter that receives the resonant frequency directly from



〈Figure 10〉 The basic structure of switching DC-DC converter

wireless power transmission system, DC-DC converter is operated in synchronization with the internal clock. At this time, driving power loss is not large because it generally operates at a lower frequency than the resonance frequency. Therefore, it is advantageous to use nMOS power transistor. Likewise with AC-DC converter, if switching frequency of DC-DC converter sets higher in order to reduce the size of the power inductor, it is better to use a schottky diode may be more advantageous in terms of efficiency.

〈Fig. 10〉 shows a basic structure of switching DC-DC converter that by applying high side switch to pMOS transistor and by applying low side switch to nMOS transistor. It amplifies the difference between VFB voltage and VBGR reference voltage which were divided output voltage by resistor R1 and R2, and adjusts the duty that pMOS and nMOS power transistor are turn-on by comparing it to the ramp signal VRAMP. Through this process, the output voltage of the DC-DC converter can be regulated. At this time, the dead time control plays a role to prevent the short circuit of input voltage VIN and GND by both power transistors are turn-on at the same time.

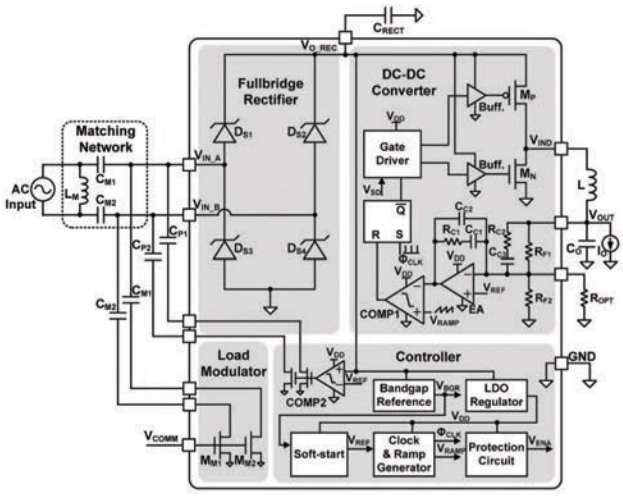
3. The battery charger

If electronic devices that wireless power transmission is applied, which operates with power from a battery, then a circuit for charging a battery is additionally required. The type of the battery charging circuit is linear battery charger and switching battery charger as in DC-DC converter of wireless power receiver. Portable devices such as the latest smartphones apply switching battery charger for most in order to maintain high power efficiency and to alleviate the problem of heat generation. As the DC-DC converter of wireless power receiver operates by comparing output voltage with reference voltage, in the case of the battery charger, it operates on the principle of comparing output current with reference voltage. Since the principle of operation of the other blocks is the same, battery charger and DC-DC converter may be configured as a single block when designing wireless power transmission system. This makes it possible to improve the overall efficiency of wireless power system.

4. The protection circuit

Wireless power transmission system is enclosing the danger of electric shock, heat generation and battery destruction, because it conducts power transmitting and receiving. The protection circuit must be considered in order to solve and to remedy these problems. The first matter to be considered a case the excessive power transmits to wireless power receiver. Supposing an initial environment of wireless power transmission, if it is in the state of power is not being properly supplied to the battery, there will be a possibility that excessive power is supplied to wireless power receiver. Excessive power may also be supplied to wireless power receiver upon switching multi charge into single charge as well.

This phenomenon can destroy schottky diodes of AC-DC converter and transistors. In order to solve this problem, technique to limit the transmitted power excessively is required. In addition, temperature protection circuit is needed in wireless power transmission system. Power loss occurring in the situation of receiving or transmitting power, is generating heat, thus, increased temperature which can cause incorrect operation, and may damage circuits and elements. When the temperature of the wireless power receiver is excessively increased, the best solution is to reduce the amount of power to be transferred from wireless power transmitter. In order to apply this technique, wireless power receiver is able to communicate with wireless power transmitter. Furthermore, overvoltage and overcurrent circuit are required to prevent voltage and current of the circuit exceed the tolerance level as well as overpower and temperature protection circuit.



〈Figure 11〉 Block diagram of developed wireless power receiver

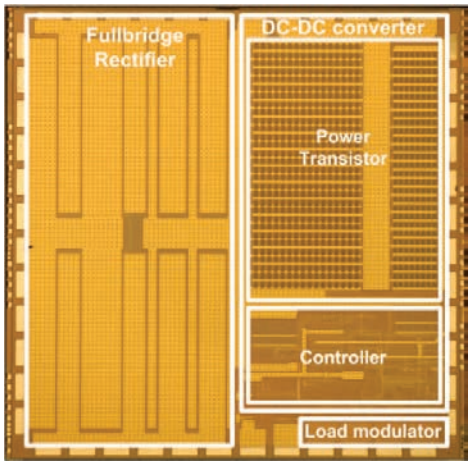
Ⅲ. The development case of wireless power receiver

〈Fig. 11〉 shows a block diagram of wireless power receiver has been developed as an integrated circuit. This development case is the content that was presented at 2012 european microwave conference, part of it will be introduced below. AC-DC converter was composed of four Schottky diodes and one external capacitor. Simulations of applying schottky diode at its resonant frequency found that was possible to obtain a higher efficiency than an active rectifier. The resonance frequency of the wireless power receiver is 13.56MHz in ISM band frequency, the simulation was carried out in the final output transmission state of 2.8W. It is rectified into DC voltage by AC-DC converter, and then, stable voltage is supplied to the battery charger through DC-DC converter.

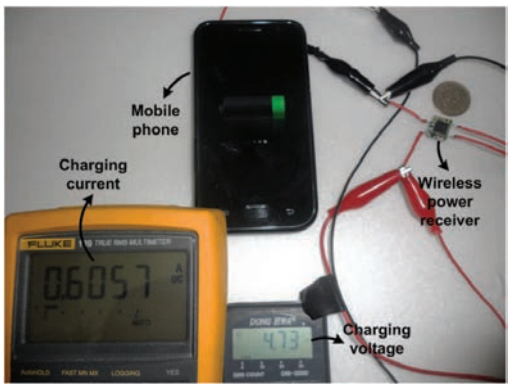
DC-DC converter employs the pMOS (nMOS) transistor of high (low) side switch. When using the high side switch as nMOS power transistor, an external capacitor is required to implement a bootstrap driver circuit. Thus, it puts emphasis on the form-factor, and then pMOS power transistor are used. The DC-DC converter employs the conventional voltage-mode control scheme with type-III frequency compensation for the fast transient response.

Maximum supply voltage of internal control circuit of switching DC-DC converter is 5V, whereas input voltage of DC-DC converter is 5.5V~12V, therein lies low-dropout regulator, and it generates and supplies 5V for internal control circuit. And included a bandgap circuit in order to obtain a stable output voltage. Then, in the initial operation state of DC-DC converter, excessive current may flow through the power inductor or power transistor, therefore a soft-start circuit is included to prevent them.

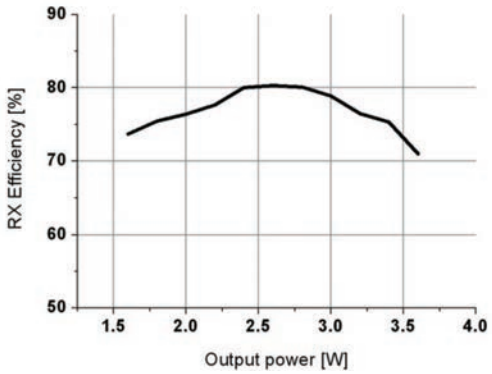
An excessive power protection circuit is also includes to prevent a phenomenon of excessive power input. If output voltage of the rectifier rises above the reference voltage due to excessive power is supplied to the rectifier, output of comparator COMP2 is high. As a result, input voltage VIN_A, VIN_B and capacitor CP1, CP2 are placed respectively in grounds. Impedance mismatch between the resonator and the wireless



〈Figure 12〉 Photograph of fabricated integrated circuit chip



〈Figure 13〉 The measurement environment of wireless power receiver



〈Figure 14〉 Measured efficiency of wireless power receiver according to the output power

power receiver will happen by this, so that received power is reduced. Over temperature, over voltage and over current protection circuit were included, it prevent the proposed integrated circuit is damaged.

It included a load modulator for enabling communication between wireless power receiver and wireless power transmitter. When the data for communication is input to the node VCOMM, capacitors CM1 and CM2 are connected or unconnected to the resonator, thus the impedance is adjusted. Then, impedance matching or mismatching of resonance coil of wireless power transmitter and wireless power receiver occurs. This is to be restored through envelop detector in wireless power receiver.

Photograph of fabricated integrated circuit chip is the same as in 〈Fig. 12〉, and the measurement environment is shown in 〈Fig. 13〉. The measurement was conducted in following condition: wireless power resonance frequency was 13.56MHz, the output voltage of DC-DC converter was 4.7V and charging current was 600mA. AC-DC converter is connected to a capacitor having a 100μF, the input voltage of the converter may have a value of 4.0 ~ 8.0VAC,RMS.

Power inductor of switching DC-DC conductor is 10μH and has a series resistance of 100mΩ. The switching frequency is 1MHz and the input voltage may have a value of 5.5V~12V. Switching DC-DC conductor was measured that has 92% efficiency in the output transmitting state of 2.8W. Overall efficiency is measured at 80% in the output transmitting state of 2.8W, the efficiency of the wireless power receiver according to the output power is shown in 〈Fig. 14〉.

Ⅳ. Conclusion

Up to now, research of wireless power transmission system and design method for each block have been introduced. Wireless power transmitter is composed of AC-DC converter and DC-AC converter, it is most important to design DC-AC converter having a high efficiency. And wireless power receiver is composed of AC-DC converter and DC-DC converter, it is important to design high efficiency AC-DC converter at high resonant frequency. Then, development case of wireless power receiver for mobile phone charging was introduced.

Thanks to

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Error Control Methods for Low-voltage, Low-area Embedded Memory


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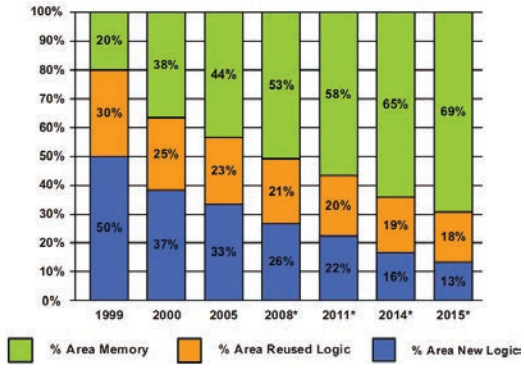
Ⅰ. Introduction

Embedded memory is used for Cache or Buffer with goals of storing a large amounts of calculated data or achieving high throughput processing in semiconductor chip such as a mobile Application Processor(AP), Graphic Processing Unit(GPU), Digital Signal Processor(DSP). With scaling CMOS process technology the capacity of embedded memory in processor has grown till now and it's expected to be continued[1]. 〈Fig 1〉

The embedded memory which has rapidly increasing capacity is showing increased error rate resulted from shrinking process technology. The refined technology of CMOS manufacturing process, which reduces manufacturing costs per chip, induces increased variation in transistors' size. This increases error rate in chip operations due to unintentional change of P/N ratio (PMOS/NMOS). Also transistors fabricated with refined process technology shows more vulnerabilities to high energy neutron, Alpha particles or electromagnetic interference such as noises from external power supply. The errors induced by reasons of the former case is called as "soft error", which usually happen in occasional situation but the "hard errors" are mostly determined at the fabrication process so the hard error decides cell's permanent characteristics. In this article error correction codes and other countermeasures to cope with these two types of errors will be introduced briefly. Especially



〈Figure 1〉 Increasing capacity of embedded memory

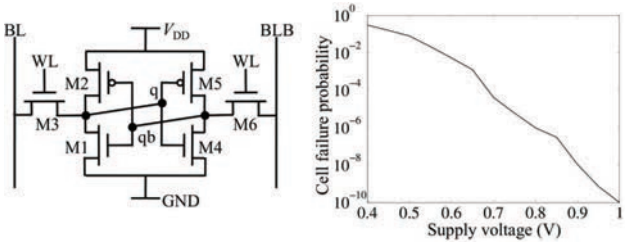
it'll be introduced in two areas such as General processor memory and DSP memory along with countermeasures for error correction codes.

Ⅱ. Embedded Memory Failures

The increasing problem of process variation is becoming a serious obstacle for SRAM's stable operation. Especially in trends of lowering power consumption through supply voltage scaling, error occurrence tends to be increased. By the process variation acquired through the Monte-Carlo simulation, 〈Fig. 2〉 refers bit error probability of 6T SRAM using 45nm PTM.[2] With the lowered supply voltage, as shown in the figure, error occurrence probability is greatly increasing in 6T SRAM.

It could incur fatal operational failures to processor operations with error occurrences in registers or caches of general processor. For example, when errors occur in instruction code of register or data such as tag information will ruin the intended operations. So memories used for General Processor especially requires higher reliabilities.

In case of DSP processor, it's similarly unavoidable to huge quality degradation in whole



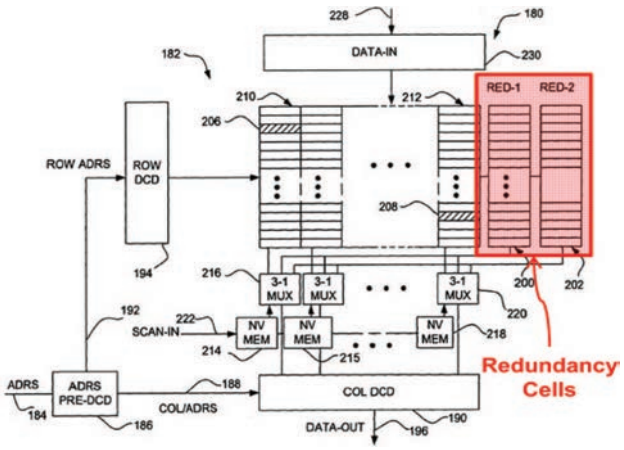
〈Figure 2〉 Error probability of 6T SRAM under Low-voltage Operation (45mm PTM Process)

system when significant level of error occurrence take place. But, because the DSP processor operates along with a specific algorithm, predetermined importance differences of data in memory can be considered. For example, a case of errors caused in Higher priority order bit(HOB) has more serious quality degradation of stored information than a case of errors caused in lower priority order bit(LOB). Likewise, considering importance of data in memory, we can get more efficient error control methods.

Ⅲ. Countermeasures for Memory Errors in General Processor

1. Countermeasures for Hard Error

Hard error means a kind of errors causing in bad cell occurred from the process variation. A faulty cell or word data which includes the faulty cell has much higher possibility of permanent hard errors. To prevent frequent error occurrence from bad cell, the Built-in self-test(BIST) circuit as shown in the 〈Fig. 3〉 has been researched and employed.[3] These circuits are inserted with embedded memory and identify bad cell before the main operations of memory. As shown in the figure, BIST circuit the prevent memory writing or reading on cells identified as faulty cells using information of identified malfunction cell.



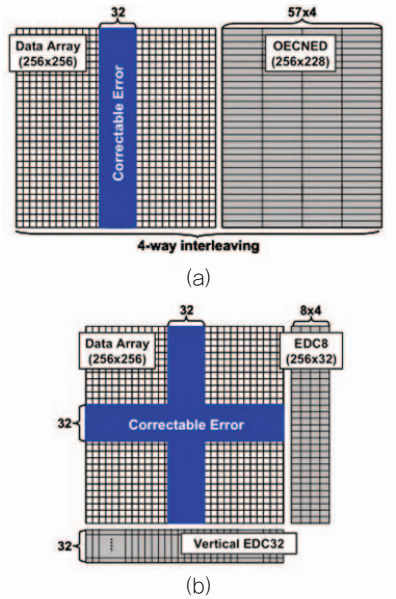
〈Figure 3〉 BIST circuit containing redundant memory cells

2. Countermeasures for Soft Errors

Soft errors occurs unpredictably by various reasons such as alpha particle impingement or noises from electric source voltage or changeable temperature by increasing running time. So the countermeasures for hard errors mentioned above is not effective when applying it to the soft errors. Generally, these unpredictable errors requires error correction code which additionally requires spare parity to correct errors when errors caused within a certain level. Error correction codes for the embedded memory are classified along with their complexities into 1)Parity check code, Repetition code, 2) Hamming code, 3) BCH code. Due to the unpredictable occurrence frequency of soft errors the error correction code usually uses spare memory with a criteria for the worst case of error occurrence. So the existing error correction code has some problems such as big area overheads from spare memories and from the decoder hardware. It also should be considered to reduce decoding latency when memories such as caches require high speed operation in the circumstances of increasing latency of stronger error correction code decoding.

a. Two-dimensional Error Correction Code

By impingements of high energy neutron or alpha particles in memory core area in which transistors are especially dense, more data stored in the area could be destroyed by influence of alpha particles, which is called as "Bust error". As a result, increasing number of adjacent cell influenced by alpha particle impingements and it requires higher error correction capability. The existing error correction codes have responded to strengthen error correction capability in situations of increased error occurrence, which incurs a large overhead. The two-dimensional error correction code is proposed to cope with these errors[4]. The two-dimensional error correction reduces spare memory usage by encoding parity



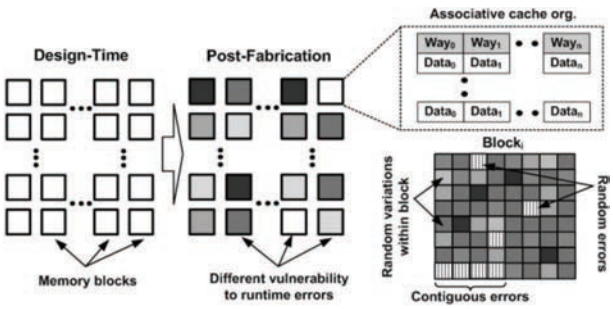
〈Figure 4〉 (a) Existing 1D error correction code and its redundant memory of error correction code. (b) 2D error correction code and redundant memory

check code into coded data in two-dimension. The parity check code can't conduct error correction by adding small spare memory but only can notice some error occurrences.

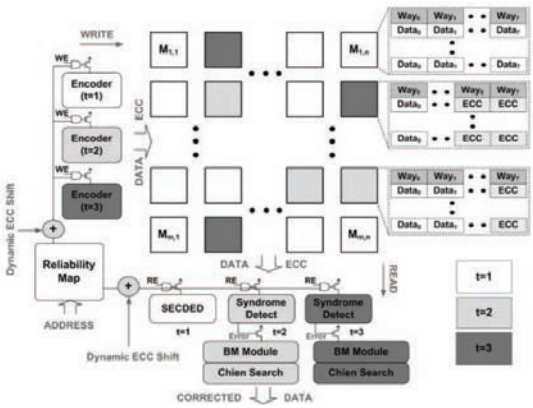
It's impossible for the parity check code to correct errors in a case of encoding with single direction but possible to find error positions(X, Y) with post-processing method in case of encoding of 2D ECC. It show us better error correction ability or similar to 〈Fig. 4(a)〉 in cases of usage of 2D error correction code structure with EDC8 or in cases of usage of existing method of 8bit-correction and 9-bit detection (OECNED) codes by less spare memory related only to "Bust error" of 〈Fig. 4(b)〉

b. Reconfigurable Error correction codes

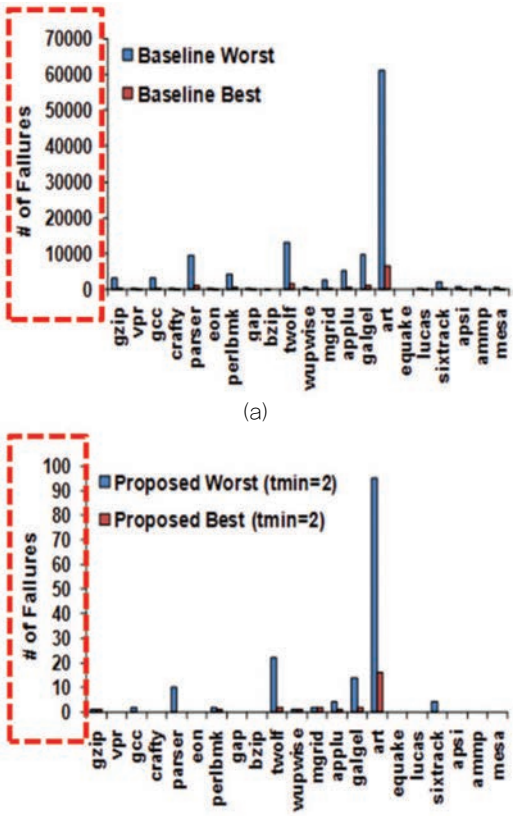
The error correction code introduced here is focusing on countermeasures for soft errors caused by regionally varying supply voltage noise or temperature or aging effect. Although every blocks were designed with equal reliability by the circuit design as shown in the 〈Fig. 5〉 the reliability of each memory block can be different from the different circumstances of the blocks. These reliability differences become worsen by refined design process and lowering of operating



〈Figure 5〉 Reliability differences and Associative architecture of Cache organization



〈Figure 6〉 Reconfigurable error correction codes decoder H/W method coping with spatial reliability differences of memory blocks



〈Figure 7〉 Comparison of the number of occurred error (a) Baseline processor using existing SECDED (b) Reconfigurable error correction codes[5]

voltage. The article[5] noticed inter- or intra- die variations and found memory blocks of cache in

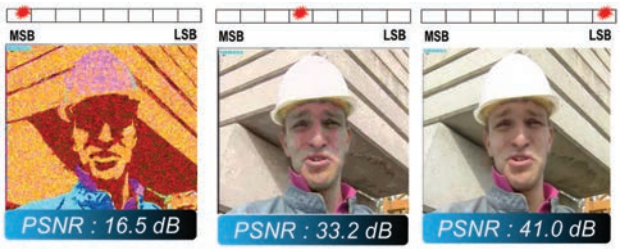
each other area have different reliability to each. It designs encoders/decoders of error correction codes which have various capabilities of error correction at the circuit design stage and uses encoder/decoder in accordance with the reliability of each blocks like 〈Fig. 6〉.

This assignment of reconfigurable error correction needs changeable storage space for changing code structures. The article[5] uses "ways" in associative cache for assignment of storage space like reference article[6] and mentions at least one or two of sacrifices of "ways" did not influence heavily on the overall performance degradation(less than 4%).

In the case of baseline processor using Single Error Correction Double Error Detection (SECDEC), it's confirmed that when a bit error probability is 10-4 many number of errors remained as shown in the 〈Fig. 7(a)〉 and when use reconfigurable error correction codes of t_{min}=2 it was confirmed that lesser errors are remained as a decoding result of 99.8%.

Ⅳ. Countermeasures for Errors occurred in embedded memory of Digital Signal Processor (DSP)

This section introduces various error countermeasures which are adaptable to embedded memory in DSP which needs a high capacity embedded memory to store many computation values of a complex algorithm and it's different from memories being used for General processor in a point that importance of each data was already decided clearly from the design because it is only used for the specified algorithm.



〈Figure 8〉 Image quality degradation from the error occurred at each bit location of 8 bit digit of H.264 Encoder

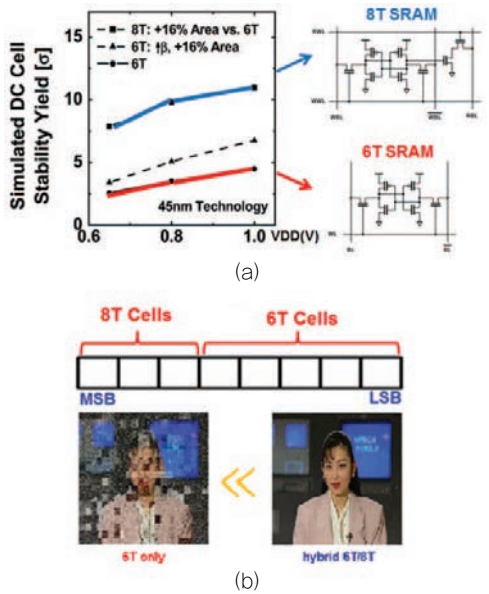
In countermeasures for errors in embedded memory of DSP the importance differences of bits stored in memory cell is used significantly. For example, in a case of error occurrence in each location of embedded memory of H.264 as shown in 〈Fig. 8〉, when errors occur in higher order bit(HOB) the PSNR indicating a criteria of image quality was lowered 42.5dB to 16.5dB comparing with non-error case.

Researches coping with the error occurrences in the embedded memory of DSP has been conducted using different influence on system quality by errors in each bit in memories. Some countermeasures for errors will be introduced briefly in the following order; 1) usage of memory circuit design, 2) countermeasures using error correction codes.

1. Method of Memory Circuit Design

a. Hybrid 6T / 8T Memory Structure Design

Two methods introduced from here are basically using the method to give higher reliability to more important data. The article [7] used 8T SRAM for more important data bit and 6T SRAM was used for less important area paying attention to stability differences and area overhead differences between 6T SRAM and 8T SRAM



〈Figure 9〉 (a) Reliability comparison with the supply voltage scaling of 6T Cell and 8T Cell (b) Hybrid 6T/8T Memory Structure construction method

〈Fig. 9(a)〉. Comparing with the reliability of 6T SRAM cell, 8T SRAM cell has higher stability in lower supply voltage but it needs more areas so it could be used for important data to reduce memory area. The hybrid memory structure using 6T SRAM and 8T SRAM was proposed and it shows us better image quality than one by memory usages of only 6T SRAM cell as shown in the 〈Fig. 9(b)〉.

b. SRAM Memory in Heterogeneous Cell Size

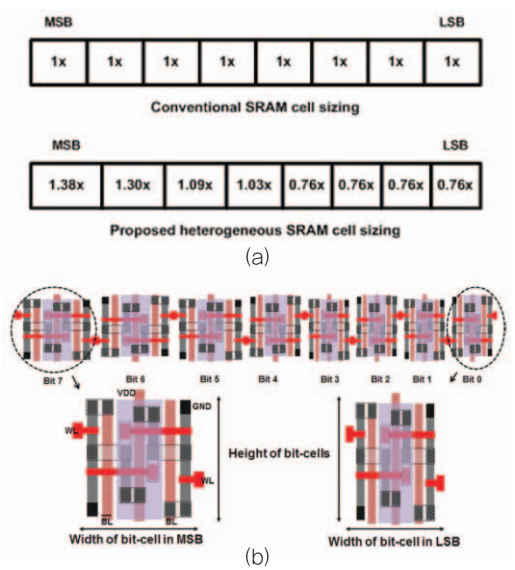
It's also possible to design structures to store important data in more stable memory cell using only the 6T SRAM cell. When errors occur in 6T memory cell, it will be influenced by process variation and increases error probability, if using bigger size of 6T SRAM cell. It will increase area overheads on the memory area when using large 6T SRAM to all data bits so the method was proposed to use more big size SRAM cells for HOB as shown in the 〈Fig. 10〉.[8]

2. Method of error correction codes.

Considering importance differences of bit data, methods of memory circuit design has been introduced so far. This section will describe effective countermeasures for increased errors using error correction codes.

a. Unequal Error Correction Codes

Unequal error correction code is composed of error correction codes in parallel structure with repetition code and Orthogonal Latin square, which is one of the simplest error correction codes.[9] These two codes have strong point of very short latency but they have another problem which needs much more spare areas. The more important data will use codes providing more strong error correction ability and less important data will use less strong error correction ability, which will be protected in that way. It's proposed



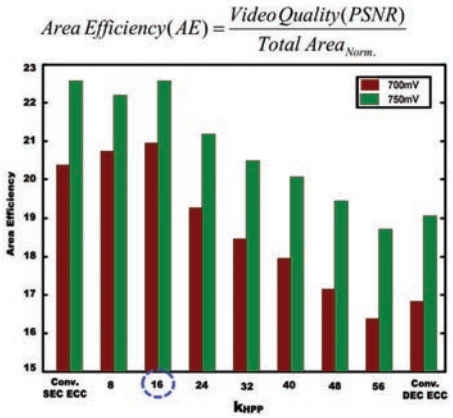
〈Figure 10〉 (a) Structure of heterogeneous 6T SRAM cell (b) Layout of heterogeneous SRAM structure

to compose unequal codes connecting codes of various error correction abilities in parallel way and searching algorithms of optimistic code composition in accordance with adapted applications.

b. Priority based Error Correction Code

Priority based error correction code[10] is composed of 1bit error correcting hamming code and 2bit error correcting BCH code in parallel to provide more strong error correction ability on more important data and provides less strong error correction capability on less important data. As shown in the 〈Fig. 11〉, area efficiency (AE) is measured as peak signal to noise ratio (PSNR) value divided by the total area including the areas of memory and encoder/decoder to compare the efficiency of each error correction codes.

The article[10] conducted simulations to gage and compare PSNRs of H.264 applying different error correction codes. In embedded memory of H.264 encoder/decoder architecture, 64 bit data word is stored in the form of 8 sets of 8 bit data constructing a word in the memory of H.264 encoder. Each case is compared with the areas of encoder/decoder and redundant memory areas which are composing 2bit error correction codes, 1bit error correction codes differently. And result values of PSNR from the simulation are compared with each other codes. The Khhp, an x-axis element, means length of data bit being protected by error correction codes of 2bit in 64bit data in 〈Fig. 11〉. The error correction code of the highest AE value is different at the different supply voltage, so the error correction code should be decided in advance in accordance with target voltage scaling level in the design process.



〈Figure 11〉 AE According to Supply Voltage Drop of H.264 Encorder

But the proposed error correction code has an weakness that the priority based error correction code can't be reconfigurably changed after composition of these codes (khhp).

c. Variable length error correction code

The variable length error correction code can change code compositions in accordance with supply voltage dropping which is different from the two previous error correction codes and so it's the key idea in error correction codes to change and protect data length by error occurrence possibilities as shown in the 〈Fig. 12〉.[11] According to the simulation results, when different error correction codes are used for embedded memory in the FFT(Fast Fourier Transfer)〈Fig. 13(a)〉, the variable length showing the highest value of code to quantization noise ratio(SQNR) is different at the different level of supply voltages as shown in the 〈Fig. 13(b)〉.

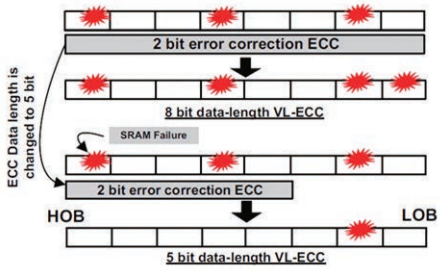
The variable length error correction code can change data length by using a singular hardware of encoder/decoder. So it's possible to select data length having better error correction effectiveness in accordance with changing supply voltage, if

the designer previously examined variable length of data which has the highest SQNR value under each of supply voltage scaling. Consequently the variable length error correction code change data length of code variably and accomplish only the highest SQNR value adapting to supply voltage. It's meaningful in a point that the article[11] induced better error correction ability in variable supply voltages using the data importance differences and pre-existing shortened ECC concepts.

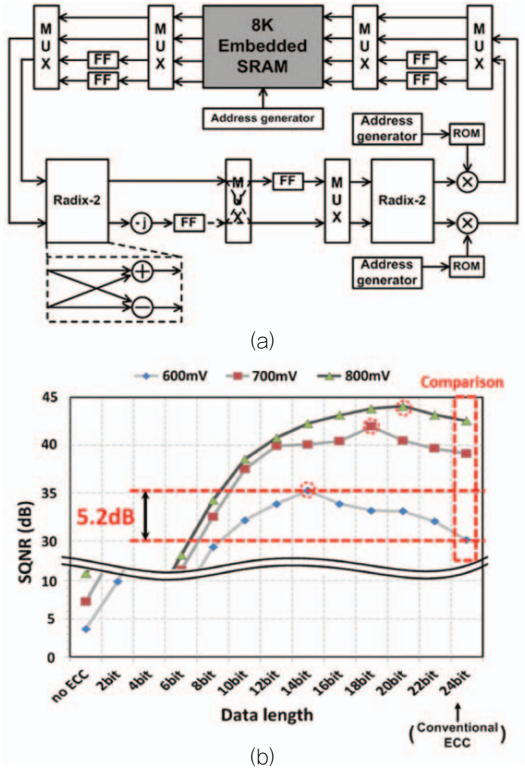
Ⅴ. Direction of Future Researches

This article briefly introduced some countermeasures for errors in SRAM mainly used in embedded memory or cache. Some pre-existing methods requires too big hardware area overheads to cope with the increasing error occurrences occurring in the refined process. To effectively deal with the increased errors, some alternatives to countermeasures for error occurrence situation have been proposed paying attention to characteristics of applications.

As previous researches have been conducted considering differences such as importance differences of bit data, reliability differences of memory blocks, the future researches will be conducted in a direction towards an error correction code development customized for a specific DSP application characteristics.



〈Figure 12〉 Handling Method for Increased Errors of Variable Length Error correction Code



〈Figure 13〉 (a) The block diagram of FFT processor and embedded memory (b) Simulation result of variable length error correction code

Because, in the past, usage of most embedded memories of high performance had been applied only in the CPU in PC, only some special companies which have technology of CPU design have developed embedded memory design to embed the memory on their processor. But by the developments of portable devices being represented with smart phone our country has a chance to jump into the application processor(AP) design and so effective usage of embedded memory should be significantly deliberated. For continuous supporting to this, our own design technology is important but we should make

abiding efforts to make error correction codes dedicated for specific application and use them effectively.

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Virtual Prototype for Early SW bring up & HW/SW co-verification

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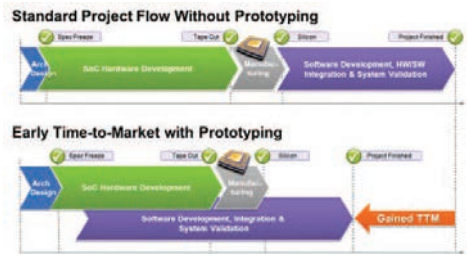
Ⅰ. Introduction

Internal standard of change of current trends that has been deformed from conventional SW to embedded SW and internal standard changes of digital devices led by Multi-core Architecture is a situation that is requesting the increase of complexity and development time of embedded SW. Through this Multi-Core Revolution, new programming language, dependency of HW / SW, a new development tool for HW team and SW team and the need of new work flow occurs. The semiconductor vendors leading current market, before starting the HW development, first accelerate development by using SW to ensure product quality and warranty, also they are using the Virtual Prototype to be able to significantly increase the number of customers.

Ⅱ. Points which claim our attention

1.1. What is a virtual prototype?

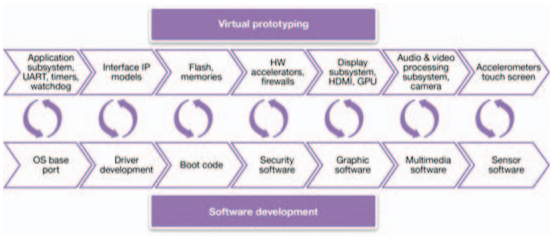
Virtual Prototype is an executable SW model of the HW



system that is running on the host computer, it simulates HW that is related to SW such as an instruction set of CPU which is the core of binary compatibility from the point of view of Virtual Prototype and SW, decoding memory map, register, interrupt and HW block. Therefore it is to be able to execute all of the SW images including ROM or firmware code, operating system and the top level SW such as AUTOSAR, middleware and applications. It provides the functions of the target system that can execute and debug in a state in which the binary program code is loaded in a similar way to SW developer is using the actual development board. However, as is discussed below, Virtual Prototype has some important differences from a physical point of view as is discussed below.

Virtual Prototype is possible to very run faster performance compared to the emulator and simulator focused on traditional HW by adjusting the details such as HW Clock cycle accuracy and low level of HW synchronization.

In addition, it has properly modeling methods according to range and complexity of the system for the compatibility of SW, in general, may require the actual development time and fewer resources smaller than the HW design is a major advantage. It also conducts properly modeling depending on range and complexity of a system



〈Figure 1〉 Software stack requirements drive the virtual prototype staging

for compatibility of SW, and in general, the main advantage is that require fewer resources and less time than the actual HW design.

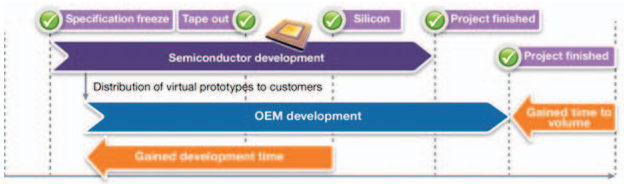
Furthermore, it can virtualized I/O of the chip including I/O interface such as main system, UAET, USB and Ethernet to create a more realistic Virtual Prototype.

For example, when installing the USB device driver, Virtual Prototype may appear to the host computer as a USB device such as a new multi-media player or a smartphone, and it can be tested at the advanced system scenario for the interface of debugger solutions that compatible with Virtual Prototype to support the existing debugging.

Another advantage of Virtual Prototype is that it can proceed SW development by generating a part of the system associated with the subset of SW stack currently under development for each step. As shown in F-1, the developer can react with increasing progressively in function of the subsystem of SW stack being developed. Also it is possible to proceed the SW development easily through the virtual architecture. For example, when porting SW to a new chip from the system-on-chip, the Virtual Prototype by upgrading the first CPU core to be able to make SW Development for new chips stage by stage because it will need to be ported to not only OS but also new CPU core. There is an advantage that it is possible to simplify the porting.

1.2. Virtual prototypes in embedded software development

Virtual Prototype can start SW development earlier than existing methods and reduce the time it takes to develop and test new products,



〈Figure 2〉 Early delivery of virtual prototypes means early delivery of finished products

besides, can proceed with HW development concurrently. (See 〈Fig. 2〉) When viewed from the perspective of SW developers who depend on FPGA Prototype or HW board, development and debugging is much easier because the HW and SW integration of Virtual Prototype because HW and SW of Virtual Prototype are integrated. It can be a direct impact on productivity with more convenient SW development, also reduces costs, resources and time significantly of SWALLOWING development, furthermore, reduces the risk of problems of product features that may occur later.

Of course, from the perspective of the HW designer, Prototype of HW development point is also necessary that can be used in conjunction with an FPGA Prototype for HW function and timing verification.

If developers want to achieve an SW functional level of 90-95%, development may begin in 9-12 months in advance possible with the criteria of an availability of silicon or physical HW availability. This has the effect of allowing designing HW in parallel with SW development and debugging.

When after HW design and verification is ready, developers can use a lot of SW stacks, and more extensive testing is also possible using HW verification technics such as HW emulation and FPGA-based prototyping. In fact, the entire product development process of this revolutionary development time by many developers are using the Virtual Prototype has been reported that more than 2-3 months is reduced. Many of the developers who are actually using the Virtual Prototype, says the entire development time of the overall product is shortened more than 2-3 months by the revolution of these development process. In addition, the integration of HW and SW makes possible to expect an improvement in productivity, can be solved up to the virtual prototype. This part has a direct impact on the business. The production of new silicon and saving delivery time that used to take 3-6 months without Virtual Prototype, but now within 3 weeks. It reduces the production development schedule risk, maintains high product quality. In addition, many developers are able to shorten the production time of new silicon and the delivery time it take existing 3-6 months to three weeks. This maintains high product quality and decreases risks for development schedule, after all, it gives a big impact on business profitability.

1.3. Virtual prototypes in embedded software debugging

Now is a phase of consuming most of the time and resources of embedded SW development because SW debugging and testing which accounted for 34% of the overall semiconductor design time by 2012, moreover, size and complexity of the SoC are increasing steadily. Therefore, it is an important issue of Embedded SW development that fixing bugs that occur in the stack of new HW architecture and new SW. Early availability of Virtual Prototype is as shown in 〈Fig. 3〉, it provides a time of 9-12 months

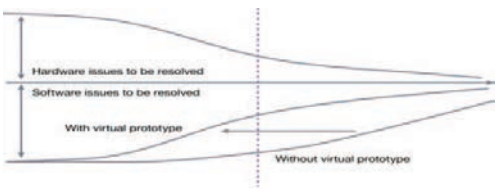
which can proceed in parallel with the HW design in the course of development and testing, thus if developers proceed tests early, definite effect appears in overall SW quality. Consequently the overall quality of products will be higher and delivery will be faster.

Through the debugging process of embedded SW using the Virtual Prototype, developers can do SW development and debugging with the following steps:

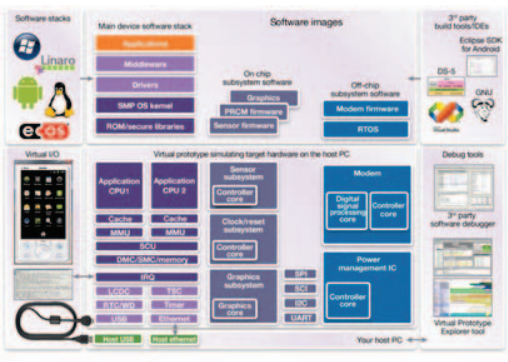
- Discovering defects
- observing defects through symptoms
- analyzing the root cause
- Reproducing the scenario
- Troubleshooting
- Re-run the scenario with the updated code to prove that defects disappeared

1.3.1. Software tool integration

As shown in 〈Fig. 4〉, Virtual Prototype provides a complete development environment of embedded SW by debugging SW components of all the ports and target devices required via actual same platform with HW. Another important element of SW development environment is an integrated part of the standard embedded SW development tool and existing workflows. In one specific case, if SW debugger solutions such as ARM DS-5, router bach trace 32 and GNU gdb



〈Figure 3〉 Virtual prototypes enable early convergence of software quality

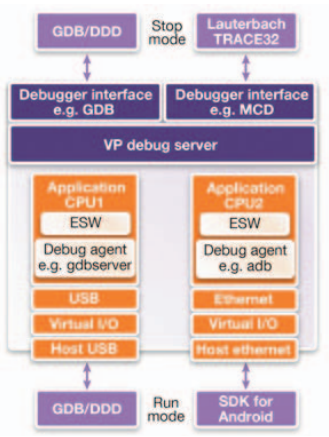


〈Figure 4〉 Virtual prototype-based software development environment

of industry-standard seamlessly integrates with Virtual Prototype, developers do not need to learn a new SW. development tools for ARM, can reduce the business for the changes to the SW.

It supports SW debug environment by way of efficient debugging scenarios as a "pause mode" and a "run mode". (Respectively, see top and bottom of 〈Fig. 5〉).

The former connects an industry standard interface such as an MCD debugging server in a virtual environment, and allows a low-level debug control on the target similar to physical target JTAG connection, and the latter is a function of Virtual Prototype which can connect virtual I/O



〈Figure 5〉 A virtual prototype in "stop" mode and "run" mode

to real world by utilizing "actual Real I/O", device drivers and physical interface of the host computer. An actual USB interface is displayed as an actual physical USB interface in the debugger, however, Virtual Prototype is not necessary to physically connect the debugger in run mode.

As a result, embedded SW development team can have a quick decision, visibility and controllability by moving SW development and debugging from an actual HW target into Virtual Prototype successfully.

1.3.2. Visibility

Another big advantage of using Virtual Prototype for debugging is that it may proceed into the code SW, HW block, the sub-system and the whole is difficult to determine the actual system when using a separate HW Block. Another great advantage of using the Virtual Prototype for debugging, SW code, HW block, sub-systems, and the actual use is the whole difficult system check at the time of the HW, carried out in separate individual Block It is the point that it is. Another great advantage of using Virtual Prototype for debugging is that it may separates whole system that is difficult to determine by individual blocks when using SW codes, HW blocks, sub-systems and actual HW. Simulation speed and visibility as well as control that is capable in the replay problems after running, are well-known advantages. Developers can check the register level of HW in Virtual Prototype, it is possible to debug the interaction problem between HW and SW. Also can configure Virtual Prototype that connecting all SW debuggers is connected to the simulator by virtue of debug server, and even if the simulation time is stopped, there is no timer tick, nor exceed the time.

In this light, SW developers can obtain a result in a more secure and consistent through securing visibility of the HW and SW, and it is possible to observe over all the boundaries such as memories and registers, as well as CPU signals, peripheral devices, subsystems, power management blocks and sensors.

Virtual Prototype users can find bugs easily by using increased visibility and control capability of Virtual Prototype, and additionally they can separate bugs from an OS and a driver.

Virtual Prototype result of user survey, when compared to the SW team of the same size, in the case of Virtual Prototype users could do more in the same resource conditions. And, it requires less resources for each project, was possible to improve productivity in the development and debugging more than 2-5 times

1.3.3. Control

When conducting SW development and debugging by using Virtual Prototype, the user can either stop the entire system, or set the interrupt without modifying memory and contents of the register, and affecting the other tasks, it is possible to continue working from that point.

1.3.4. Determinism

SW always debug environment of the Virtual Prototype characteristics to generate the same results in the same environment is very useful. And which shortens the time when users correct the defects, and provides a function capable of reproducing defect scenarios. If there is no such

a function, the SW debugging operations that is takes such a long time. For example, it is also difficult task to handle bugs that are displayed while predicting event sequence and arrive time in the scenario

1.3.5. Multicore debug

What happens when user stops a particular processor core of the actual system? The state of the system may be immediately broken due to it is impossible to stop the rest of the system. If there are multiple processors in the system, when a particular core is stopped, user is able to feel uneasy. However, even if all is stopped, Virtual Prototype users can access the system without any affect. This is because it is possible to track the processor and the status of HW entire system without moving actual data in all lock-steps. It is possible to set any breakpoints that include HW, SW and multiprocessors. Also Virtual Prototype supports multi-thread and multi-process to be able to facilitate the addition of multi-core architecture for complex problems related to the cache coherence.

1.3.6. Ease of deployment

In case of HW, supplying it to SW developers one-to-one may cause problems such as cost and time. Especially there are difficulties in cost and delivery time to provide it to SW development team from miles away.

In the case of Virtual Prototype, it can make an executable file in some sort of SW concept which enables mass replication and deliver that has a similar level with typical SW development tools. It allows delivery and redistribute the installation image of Virtual Prototype to additional SW team via e-mail or internal intranet simpler and convenient, therefore it enables the SW development work in each of the SW team without loss of significant cost and delivery time.

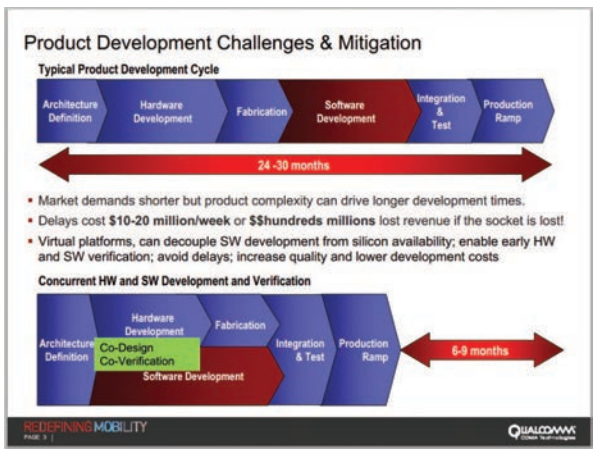
1.3.7. Fault injection

Virtual Prototype is possible to easily control the registers, on-chip, value of the signal line of the system components because it is a model of SoC or system SW. It sets the value of the register via a gui or script, and creates certain circumstances such as fault injection, may test the operation of the system under certain conditions.

It is particularly useful when developers want to test the response of the system for incorrect setting and input. Thus, it is possible to fabricate a high quality SW with automotive control function for important applications.

1.4. Validation and verification: test early, test often

Complexity of the embedded system may require to perform more tests at an earlier



〈Figure 6〉 Customer success story

phase. Virtual Prototype will allow developers to perform SW development and debugging at an earlier phase and faster time through modeling.

1.4.1. Scripting software tests

In many scenarios, it is easy to change configurations of scenario, SW and HW, also possible to perform SW test through a script based SW test.

Embedded SW in Virtual Prototype is possible to use the virtual test interface via UART serial connection.

When developers are using the virtual I/O function of Virtual Prototype, they can automates I/O devices as the user interface of Virtual Prototype such as a keypad, an LCD and a touch screen with the platform such as a host PC, a scripting and a general SW GUI test tools that is realized as a GUI. There are some advantages as follows:

- Run a better test to obtain a high quality: It is possible to test the more complex scenarios by putting the hard corner cases into the system because it offers excellent controllability and visibility from all aspects of a virtual environment system.
- Cost savings through more efficient testing: It is possible to easily configure and automate the test because the entire system is virtual and it is possible to be run on desktop PCs and server farms. For example, it is possible to debug SW in failure test faster and efficient rather than utilize existing black box technology.
- Test cost savings through extendibility: It is possible to build 1,000 test systems under various conditions through simulations. This can reduce costs and meet various test conditions.

1.4.2. Preparing post-silicon validation test software

Generally, the verification process of the semiconductor operation is, first, developing an extensive set of diagnostic test methods to verify how new silicon works as intended, and then, a fab of semiconductor supplier and post-silicon validation team to check the validity of new silicon. This flow proceeds through SW test running on various cores in typical chips. Development of test environments so far is generally can be performed in the initial physical prototypes, was possible only if the actual silicon is enabled.

Delivery of these validation test suite is one of the key elements required to ship and drive the new silicon for semiconductor vendors and customers. The use of Virtual Prototype therefore the user effectively not only can be moved to the "development of post-silicon" but also the progression of the initial verification test also possible, thus it is possible to give them a great help. Actually semiconductor vendors are using the Virtual Prototype are, a test time for product development is proceeding at an early stage has become shortened as well as bugs and operational issues of the overall product were decreased.

In addition, when developing the power management is one of the important consideration in current design, in particular, to ensure proper verification of silicon and initial SW access availability. Power consumption is a very important element in the effectiveness of the new

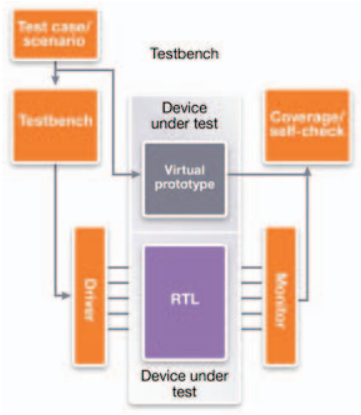
SoC. It is also not intended to be driven only by particular HW components of SoC, is used in more throughout the application SW stack. Which is controlled by the power management SW, and it cannot be obtained the results of real power and performance trade off without proper verification in the context of real-world scenarios to run the application SW and the power management SW Virtual Prototype can be helpful because it can proceed SW scenario based power analysis and debugging of the power management in early SW development.

1.4.3. Software-driven hardware verification and early hardware/software integration

Having an initial function model of HW brings the acceleration of SW development as well as more use cases of Virtual Prototype, therefore it offers benefits in many aspects. Exact function model for Virtual Prototype for being developed system, can be used in golden reference and RTL verification flow of HW platforms, therefore, it not only provides a verification concerned only with HW but an integrated verification environment in the state of HW and SW are combined.

Use Case

- Development of initial test case (test bench): RTL verification team can apply advantages of initial Virtual Prototype to accelerate the development of "system integration test". This test is the "embedded SW test" focused on SoC and IP integration issues to try to deal with IP-centric verification methodologies such as a limited random test. Virtual Prototype in this flow is a useful verification tool that can be used early in the verification.
- Virtual Prototype is used in the state of the absence of actual RTL DUT. Virtual Prototype provides a few times faster simulation speed than RTL simulation, high productivity test benches and test cases as compared to all the RTL DUT, and also the initial development is possible.
- HW / SW co-verification: When an individual IP and an RTL of the subsystem is available, it can be integrated into Virtual Prototype by using TLM / RTL integrated simulation function which can be used in an RTL simulator through an RTL model. Thus, an RTL subsystem can be tested in the whole system environment along with many of SW stacks which can be used as an advanced test case. Besides, it provides a useful cooperation environment to work between HW and SW team that performs the initial HW / SW verification of the completed product.



〈Figure 7〉 TLM/RTL co-simulation: a virtual prototype is used as virtual "DUT" to develop RTL test cases while the RTL is developed

- Generally verification team, in a state of an RTL implementation has been verified, develops "reference model" by using Golden reference and a language such as System Verilog for TLM / RTL equivalence checking.

It is possible to detect inconsistencies such as HW and SW errors, HW bugs, version differences, problems of TLM model which are derived from a variety sources, in advance by using the same model between the HW and SW. These design flows are integral parts which can provide a "Top-Down" design method that is raised from the current level of RTL. It is an important technology that can maintain the current level without increasing design and verification time due to such as an increase in design complexity and HW / SW integration.

1.5. C reating and managing virtual prototypes

1.5.1. When? The sooner the better

The most common answer for the new user of the "advantages of Virtual Prototype" was "Virtual Prototype can be applied to HW design in parallel". Today, all of the semiconductor vendors are facing with the difficulties of a very complex system, increases of silicon availability and product delivery time. Virtual Prototype can be the answer as a solution of new tools and methods that enable them to perform the work within the time limit.

If they adopt a Virtual Prototype methodology that enables the initial SW development, they may be completely maximize the advantage of being able to perform the product development according to their product development plans. For this, it will require the initial development of the model in order to construct Virtual Prototype through the initial HW specification. And, Virtual Prototype should be developed according to the needs of SW development team, consequently it will require more intimate collaboration among the teams like HW team, modeling team and SW team.

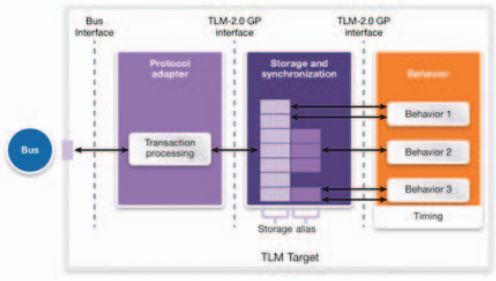
1.5.2. Building and using models

The Virtual Prototype is used as transaction level model (TLM) by using SystemC the IEEE1666-2011 standard HW modeling language.

It executes HW function rapidly with sufficient timing accuracy to enable the SW synchronization events, and constructs Virtual Prototype as a loosely timed model can debug the actual SW stack.

- TLM - 2.0 modeling using SystemC: It has been adopted to promote interoperability and uniformity of IP model, and is an industry standard of Accelera. It is the model to adopt the coding style considering the communication operation and the separation timing, and to meet the requirements of speed and visibility of the use case for a particular Virtual Prototype.

Diagram models of 〈Fig. 8〉 show each models



〈Figure 8〉 Target model coding style

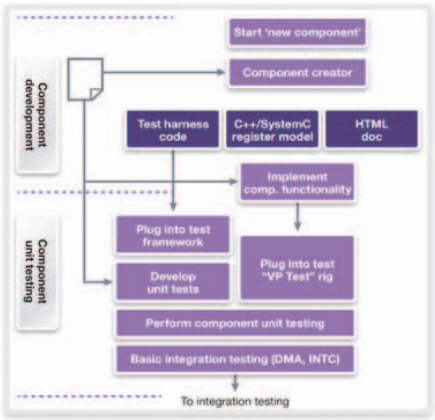
were separated and how to be designed to implement the interface.

Due to the functional separation of each component, Virtual Prototype built in each of the model can be created as a modular has been so analyzed that into small functional units or can be added gradually depending on the needs of the project

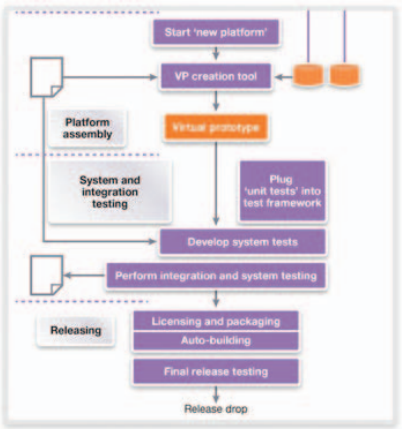
1.5.3. Leveraging test-driven development

In order to ensure the quality of the model to be used in Virtual Prototype, it is important to develop a test program in parallel with the initial model generation of Virtual Prototype. The model should be integrated into the unit test platform, when embedded SW test is added should be created so that the model exert the function of the model.

Workflow diagrams below through virtual prototyping and the modeling of the components of the release stage of the process (See 〈Fig. 9〉 and 〈Fig. 10〉) show the best way to create Virtual Prototype



〈Figure 9〉 Component Modeling Workflow



〈Figure 10〉 Virtual prototype modeling workflow

1.5.4. Market adoption and availability

〈Fig. 11〉 shows the results of market research for on Virtual Prototype solutions introduced throughout the world. Also shows the possibility of expected growth of Virtual Prototype solutions for the future.

ARM Synopsys, Inc. that provides a library representing the transaction-level models and their own semiconductor IP, is one of the leading company that supports Virtual Prototype.

Ⅲ Conclusion

Virtual prototype improves the existing flow of embedded SW development, and enabling HW / SW co-development. That is, it may be effective to shorten the overall schedule of semiconductor and system development, also can help to improve

	2012	2013	2014	2015	CAGR
Americas	29.6	33.4	36.9	41.0	11.4%
Japan	11.6	12.8	13.5	14.9	8.9%
Rest of APAC	13.5	15.5	17.7	19.6	13.1%
EMEA	10.6	10.7	11.3	12.0	4.4%
TOTAL	**65.3**	**72.3**	**79.4**	**87.5**	**10.3%**

Source: VDC Research, 2014

〈Figure 11〉 Worldwide shipments of virtual prototyping solutions by geographic region, 2012-2015 (US $M)

quality of the product by using a more rigorous test method.

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SoC Architecture Design, Emulation/FPGA Prototype, Virtual Prototype

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채용분야		응시자격
경력직	Display Analog 설계	➢ Analog 회로설계 경력자(2년 이상) 0명 ➢ LCD Driver IC 개발 경력자(2년 이상) 0명 ➢ 전문연구요원 0명
	Display Digital 설계	➢ Display IC(T-con) 개발 경력자(2년 이상) 0명 ➢ Application Engineer(2년 이상) 0명

(주)티엘아이 경기도 성남시 중원구 여수동 195 티엘아이 빌딩 7,8,9,10층 | TEL. 031-784-6800 | www.tli.co.kr

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■ **접수방법**

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■ **지원문의**

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■ **기타사항**

이력서에 지원분야, 연락처, 희망연봉 기재 필수
서류전형 합격자에 한해 면접일정 개별통보

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